Vivado从此开始（To Learn Vivado From Here）

本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用

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- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

- 内容翔实全面：涵盖Vivado所有基本功能
- 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- 描述图文并茂：给出具体操作步骤，易于快速动手实践

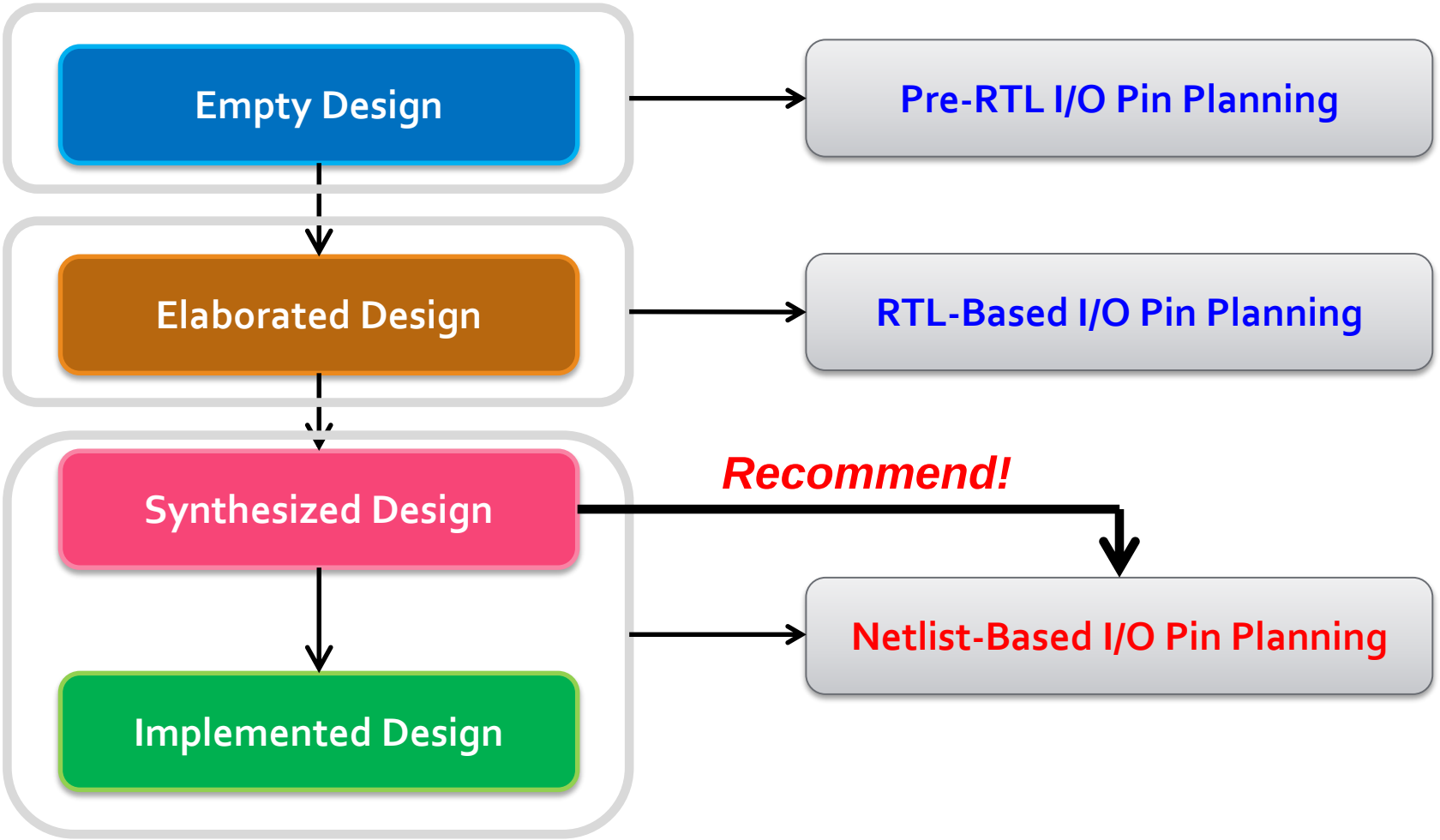
I/O and Clock Planning

Lauren Gao

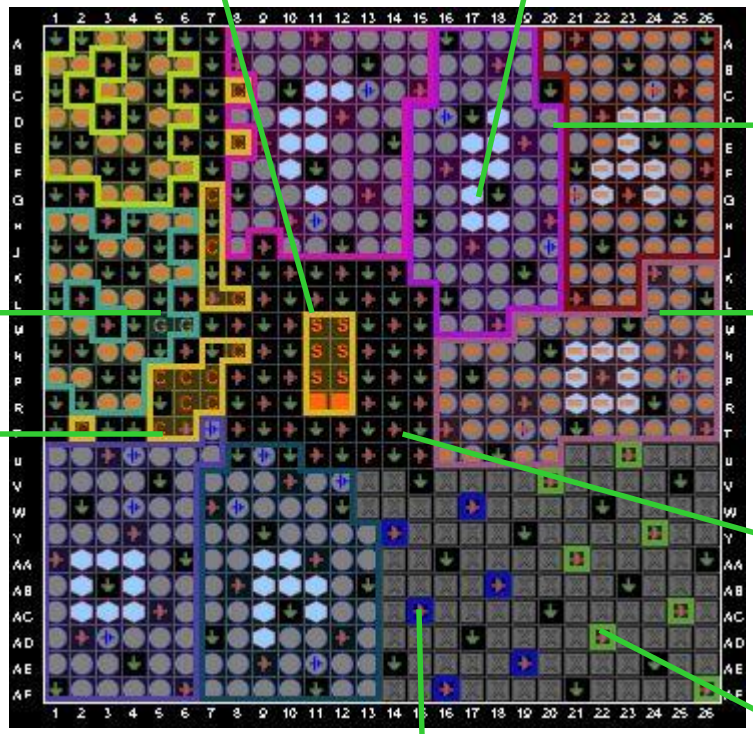
I/O and Clock Planning Overview

- **Examine and optimize I/O connectivity for PCB and FPGA design**
  - Visualize I/O and clock logic device resources
  - Consider PCB placement and device orientation, high speed interfaces
  - Align I/Os with internal FPGA resources
  - Visualize the external pins vs internal die pads relationship
- **I/O planning features**
  - Set device configuration mode and validate multi-use pins
  - Define alternate devices
  - Place I/O ports, clock logic, gigabit transceivers
- **Validate I/Os and clock assignments**
  - Visual analysis, DRC, SSN analysis
- **Interfacing with PCB designers**
  - I/O constraints, IBIS
  - Optimize connectivity

I/O and Clock Planning Stages



Package View



XADC

GND/VCC
VREFP/VERFN
VP/VN

MGT

Config

CCLK
VCCBATT
INIT_B
DONE
TCK/TMS
TDO/TDI
CFGBVS
PROGRAM_B
M0/M1/M2

MRCC/SRCC

User I/O

Occupied Pins

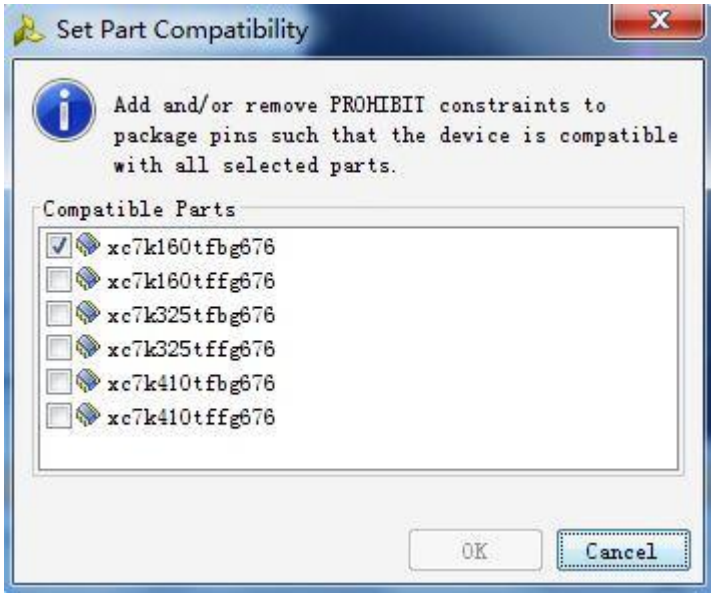
VCCINT
VCCBRAM
VCCAUX
VCCAUX_IO

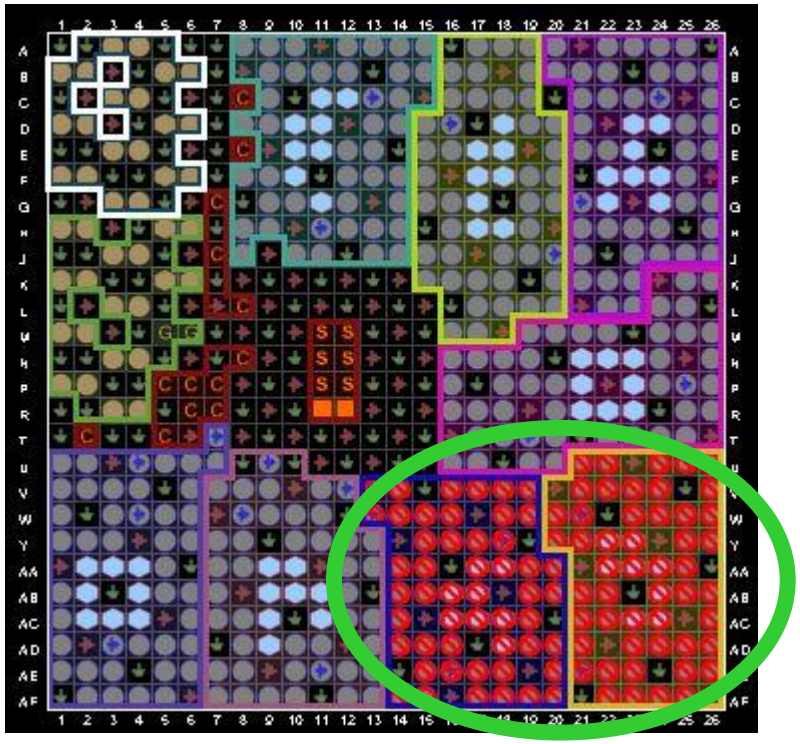
VCCO

GND

Set Part Compatibility

Tools → I/O Planning → Set Part Compatibility

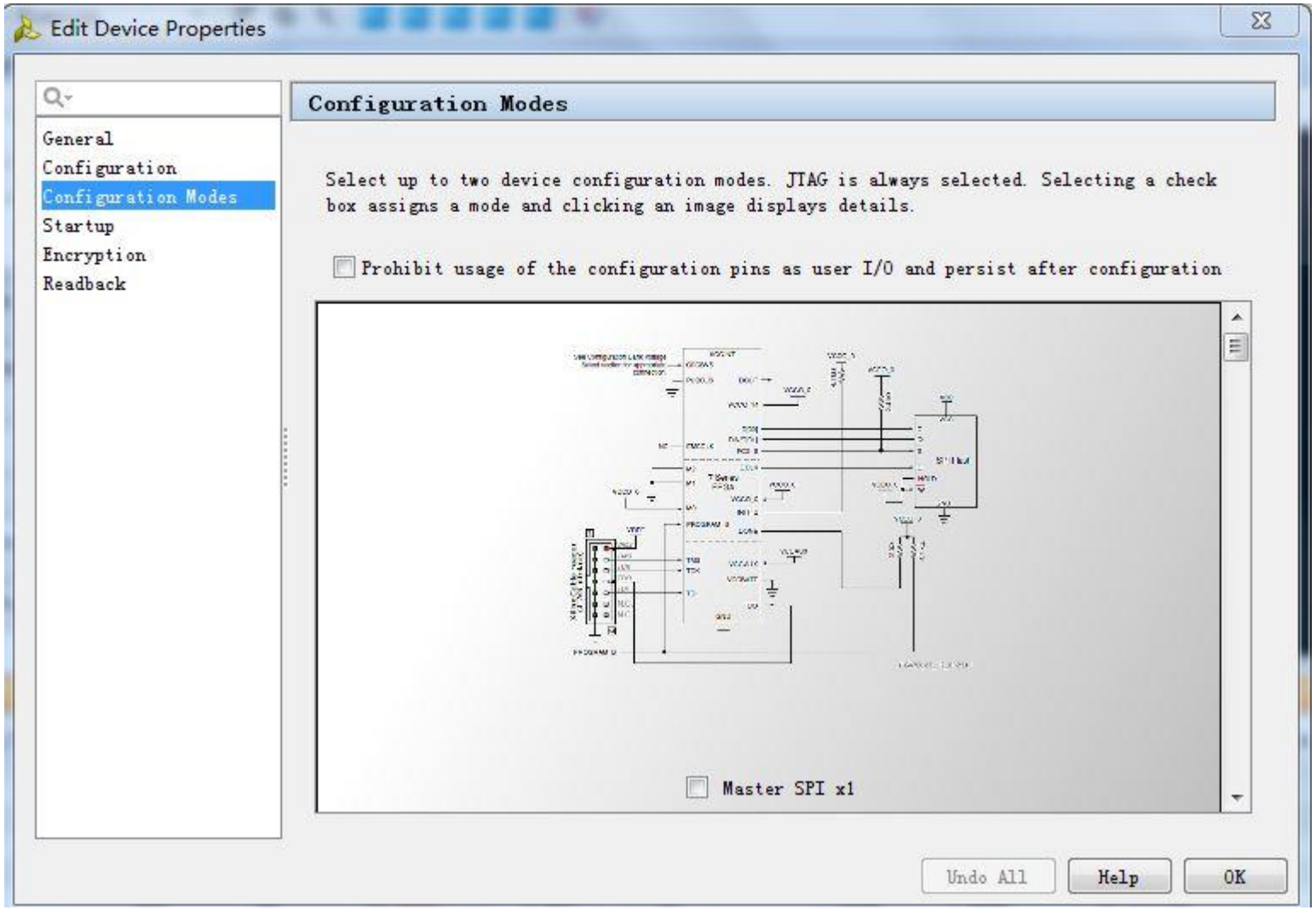




The number of pins available for placement might be reduced when you select additional alternate parts

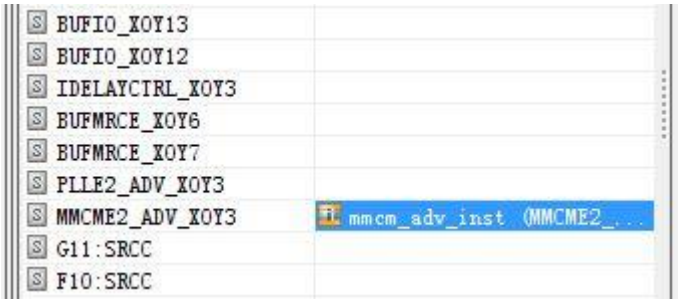
Set Device Configuration Modes

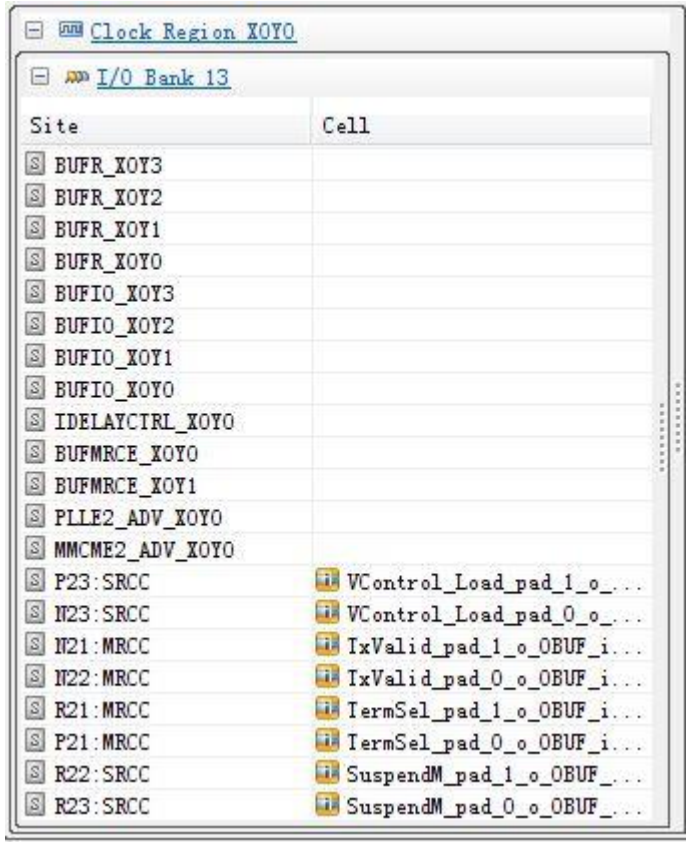
Tools → Edit Device Properties



Clock Resources

Window → Clock Resources





It is recommended that you select clocking resources prior to pin out selection

Pin Assignment from UCF to XDC

UCF

```
NET "ddr3_dq[0]" LOC = "AF7" | IOSTANDARD = SSTL15_T_DCI | VCCAUX_IO = HIGH | SLEW = FAST
```

XDC

```
set_property VCCAUX_IO HIGH [get_ports {ddr3_dq[0]}]
set_property SLEW FAST [get_ports {ddr3_dq[0]}]
set_property IOSTANDARD DIFF_SSTL15_T_DCI [get_ports {ddr3_dq[0]}]
set_property PACKAGE_PIN L13 [get_ports {ddr3_dq[0]}
```

For 7 series devices, all I/O ports must have explicit values for the PACKAGE_PIN and IOSTANDARD constraints to generate a bitstream file.

Package Pin and I/O Port Properties

Package Pin Property

Property	Type	Read-only	Value
BANK	string	true	15
BUFIO_2_REGION	string	true	
CLASS	string	true	package_pin
DIFF_PAIR_PIN	string	true	
IS_BONDED	bool	true	0
IS_CLK_CAPABLE	bool	true	0
IS_DIFFERENTIAL	bool	true	0
IS_GENERAL_PURPOSE	bool	true	0
IS_GLOBAL_CLK	bool	true	0
IS_LOW_CAP	bool	true	0
IS_MASTER	bool	true	0
IS_VREF	bool	true	0
IS_VRN	bool	true	0
IS_VRP	bool	true	0
NAME	string	true	B18
PIN_FUNC	enum	true	VCCO_15
PIN_FUNC_COUNT	int	true	1

Port Property

Property	Type	Read-only	Value
CLASS	string	true	port
DIFF_TERM	bool	false	0
DIRECTION	enum	false	IN
DRIVE	enum	false	12
HD.ASSIGNED_PPLOCS	string*	true	
HOLD_SLACK	double	true	needs timing update***
IN_TERM	enum	false	NONE
IOBANK	int	true	14
IOSTANDARD	enum	false	LVCMOS18
IS_GT_TERM	bool	true	0
IS_LOC_FIXED	bool	false	1
KEEPER	bool	false	0
LOC	site	false	IOB_X0Y78
LOGIC_VALUE	string	true	needs timing update***
NAME	string	false	sysClk
OFFCHIP_TERM	string	false	NONE
PACKAGE_PIN	package_pin	false	D23
PULLDOWN	bool	false	0
PULLUP	bool	false	0
SETUP_SLACK	double	true	needs timing update***
UNCONNECTED	bool	true	0

DEMO