Vivado从此开始（To Learn Vivado From Here）

本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用

作者：高亚军（Xilinx战略应用高级工程师）

- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

- 内容翔实全面：涵盖Vivado所有基本功能
- 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- 描述图文并茂：给出具体操作步骤，易于快速动手实践

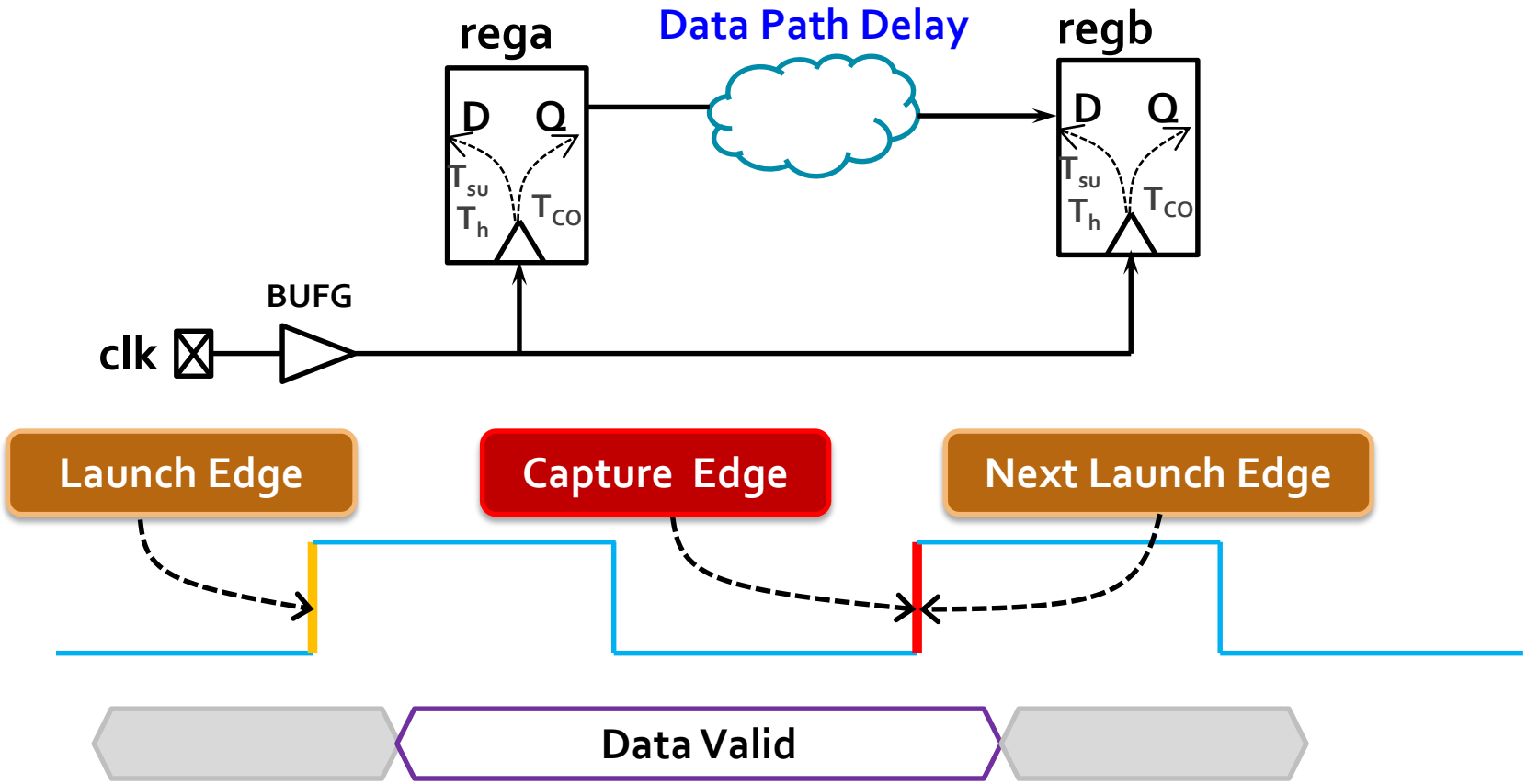
Basic Concept and Terminology of Timing Analysis

Lauren Gao

Agenda

- Launch edge vs. Capture edge
- Timing path
- Data arrival time vs. Data required time
- Setup slack vs. Hold slack

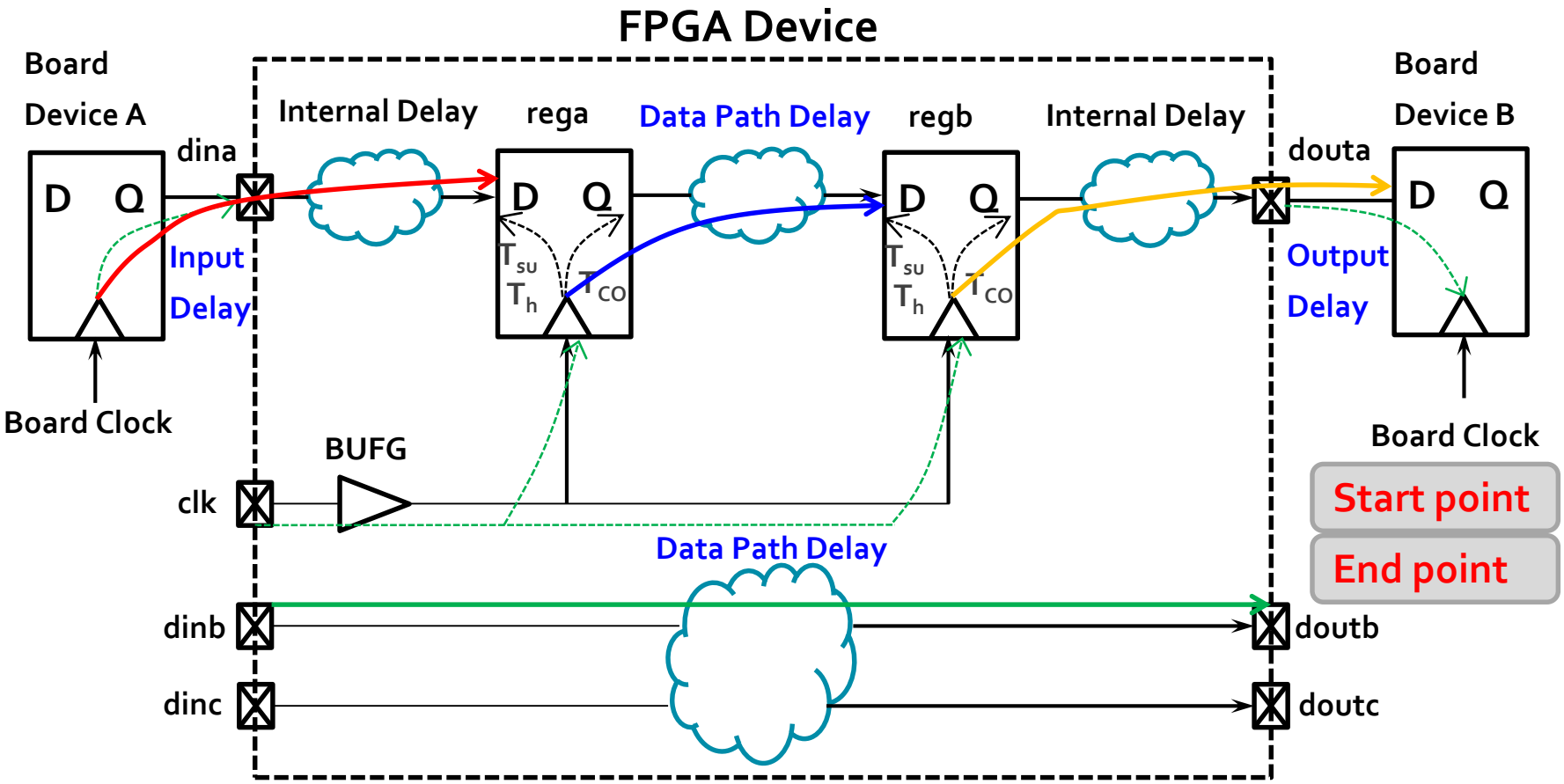
Launch vs. Capture Edges



Launch Edge : the edge which "**launches**" the data from source register

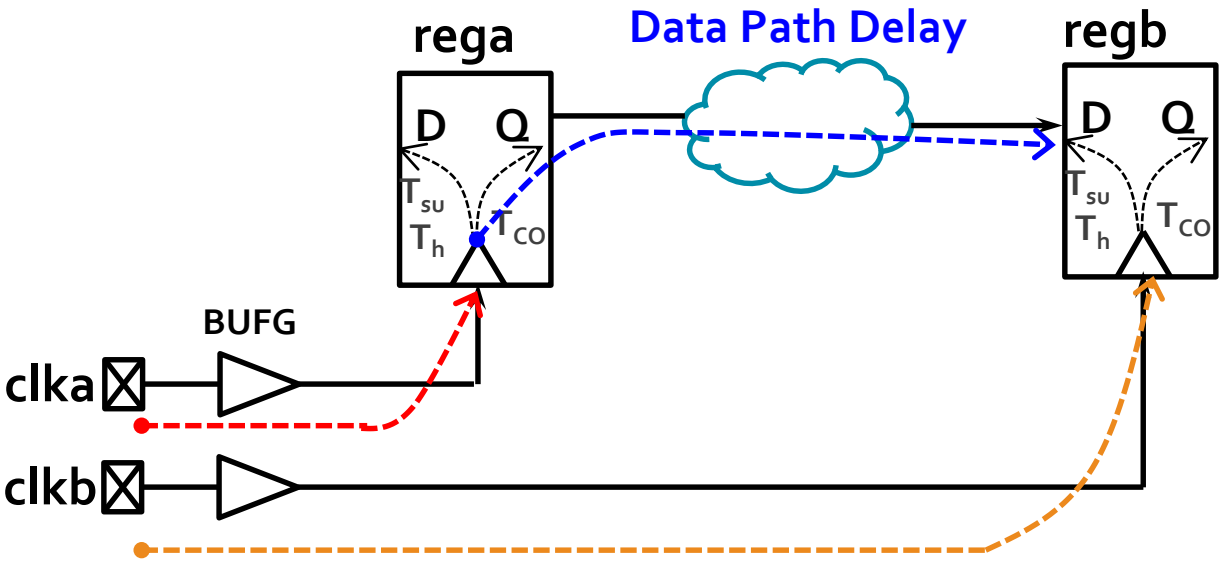
Capture Edge : the edge which "**captures**" the data at destination register (with respect to the launch edge, selected by timing analyzer; typically 1 cycle)

Four Types of Timing Path



Input Port to Internal Sequential Cell Path	S	DeviceA/clk	E	rega/D
Internal Path from Sequential Cell to Sequential Cell	S	rega/clk	E	regb/D
Internal Sequential Cell to Output Port Path	S	regb/clk	E	DeviceB/D
Input Port to Output Port Path	S	input	E	output

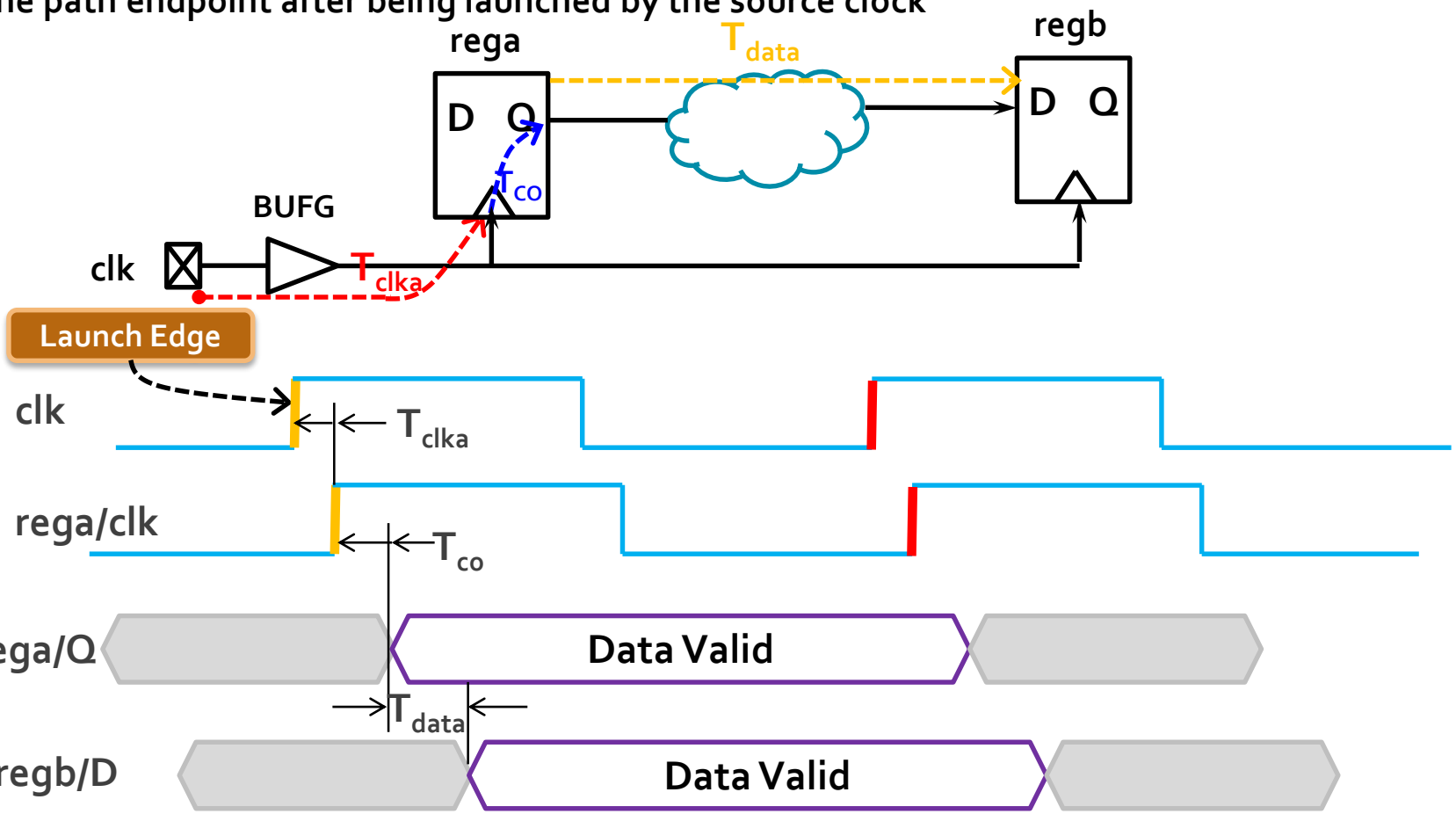
Timing Path Sections



Path	Start Point	End Point
Source Clock Path	Clk input port	Clk pin of launch reg
Data Path	Clk pin of launch reg	Data input pin of capture reg
Destination Clock Path	Clk input port	Clk pin of capture reg

Data Arrival Time

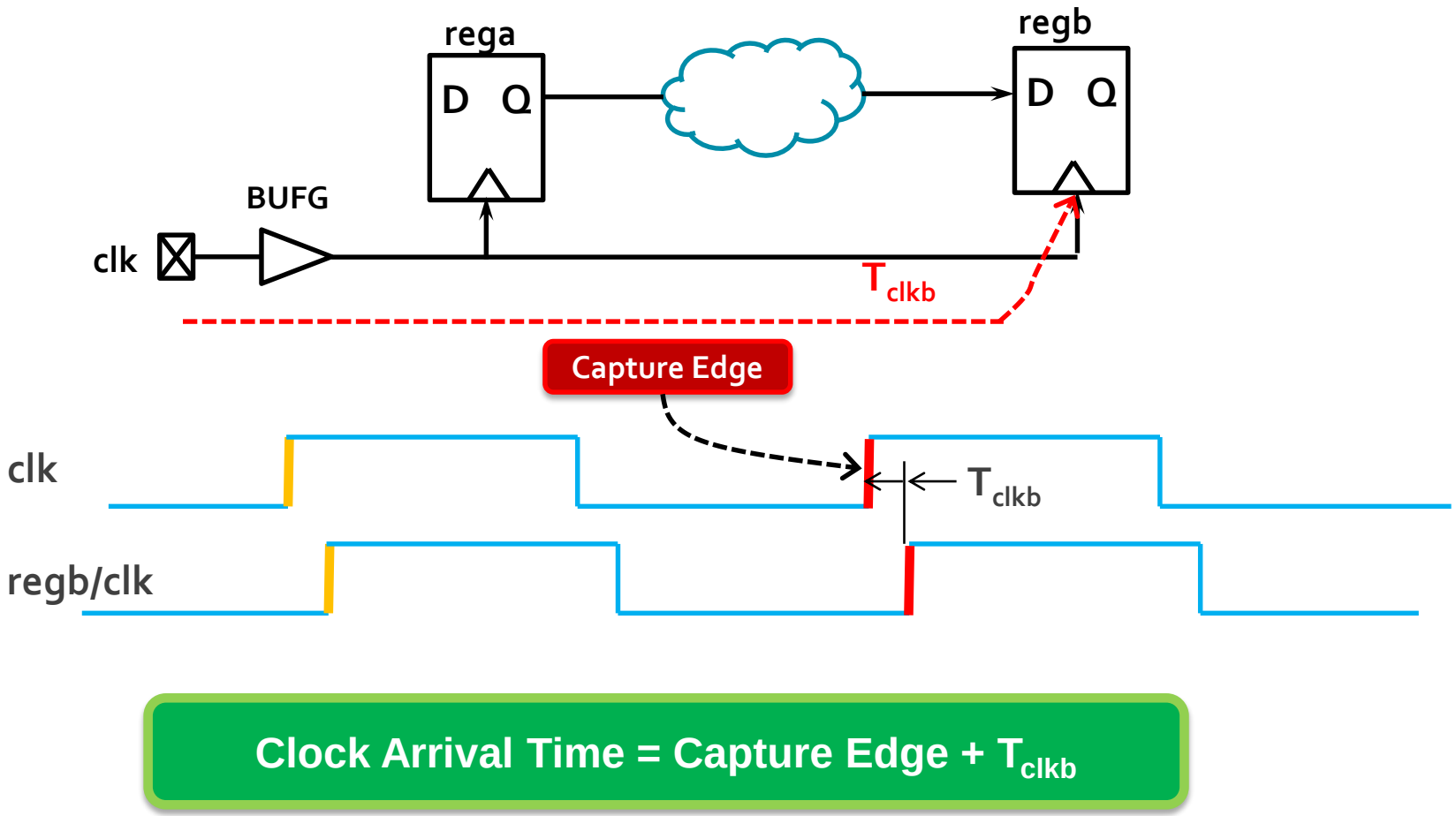
The data arrival time for setup analysis is the time it takes for the data to be stable at the path endpoint after being launched by the source clock



Data Arrival Time = Launch Edge + T_{clka} + T_{co} + T_{data}

Clock Arrival Time

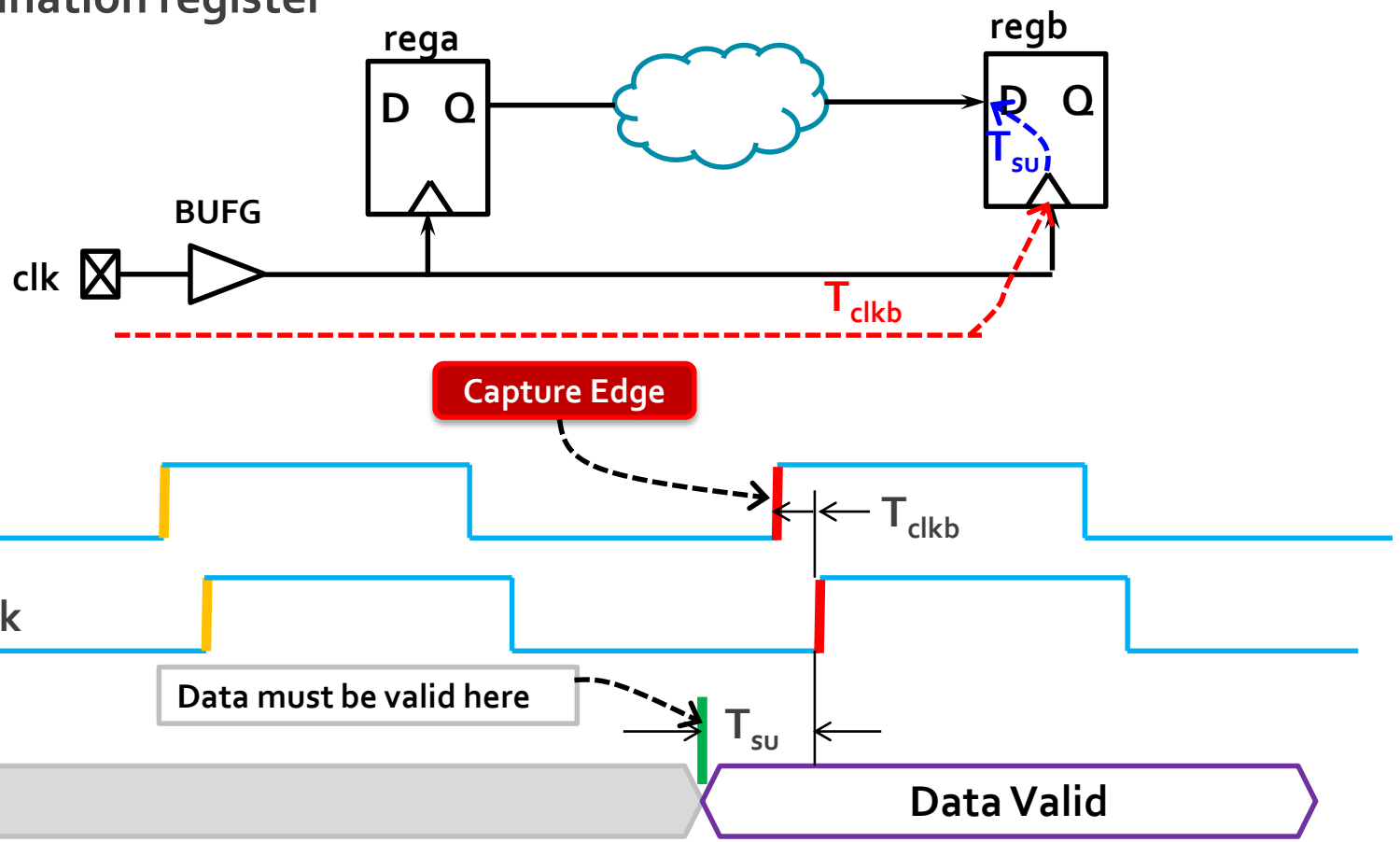
The time for clock to arrive destination register's clock input pin



Clock Arrival Time = Capture Edge + T_{clkb}

Data Required Time – Set up

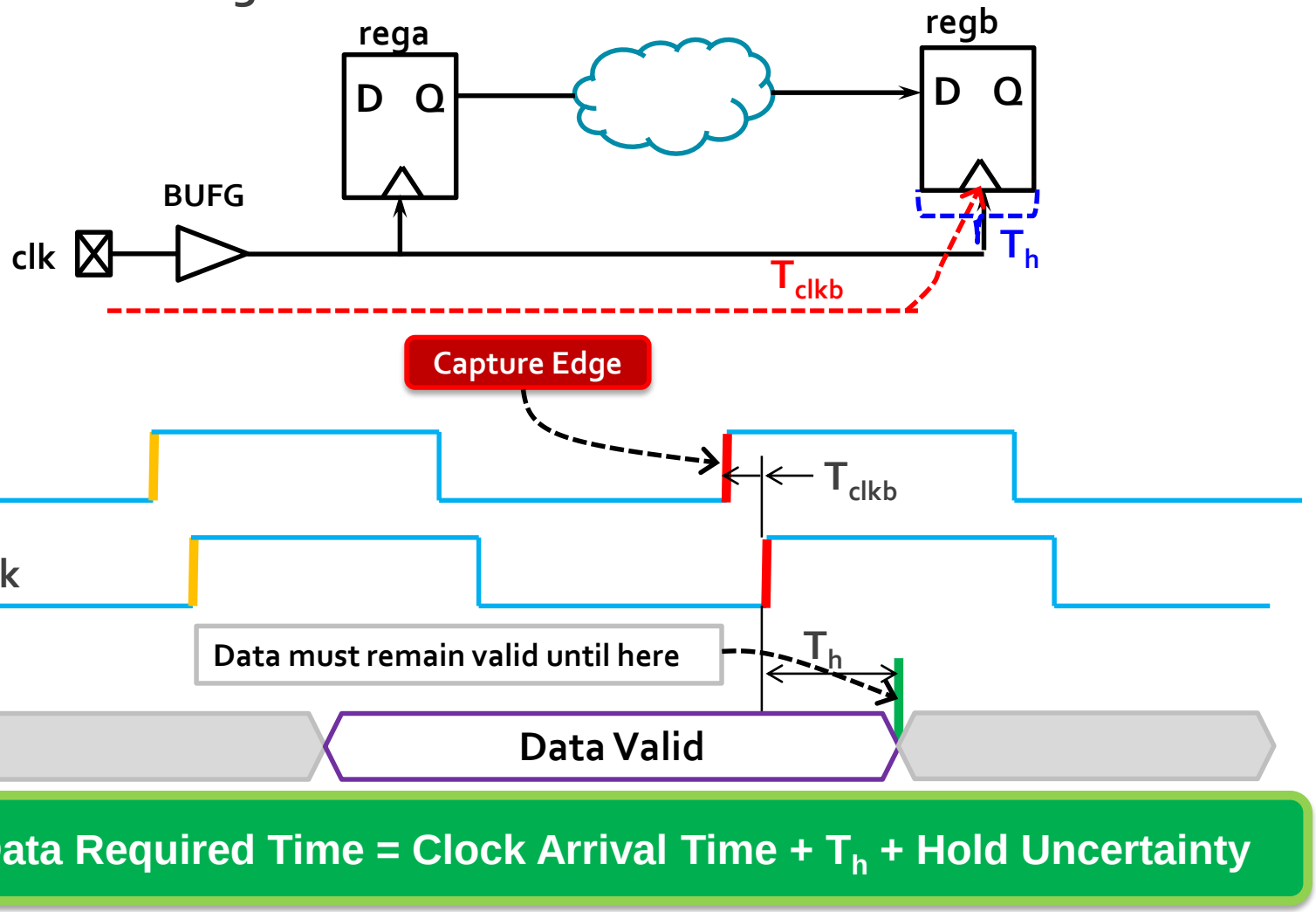
The minimum time required for the data to get captured by the destination register



Data Required Time = Clock Arrival Time – T_{su} – Set up Uncertainty

Data Required Time – Hold

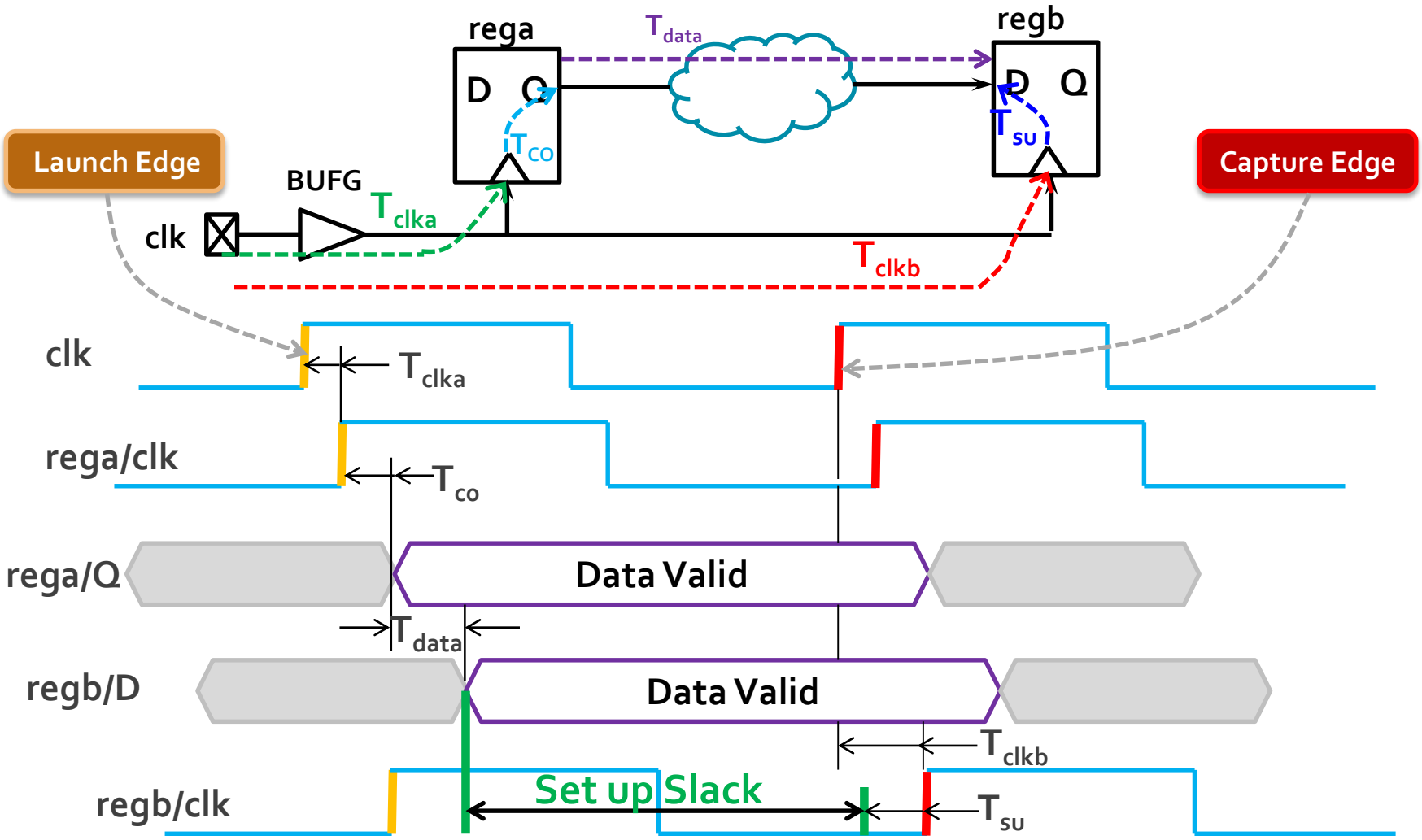
The minimum time required for the data to remain stable after captured by the destination register



Data Required Time = Clock Arrival Time + T_h + Hold Uncertainty

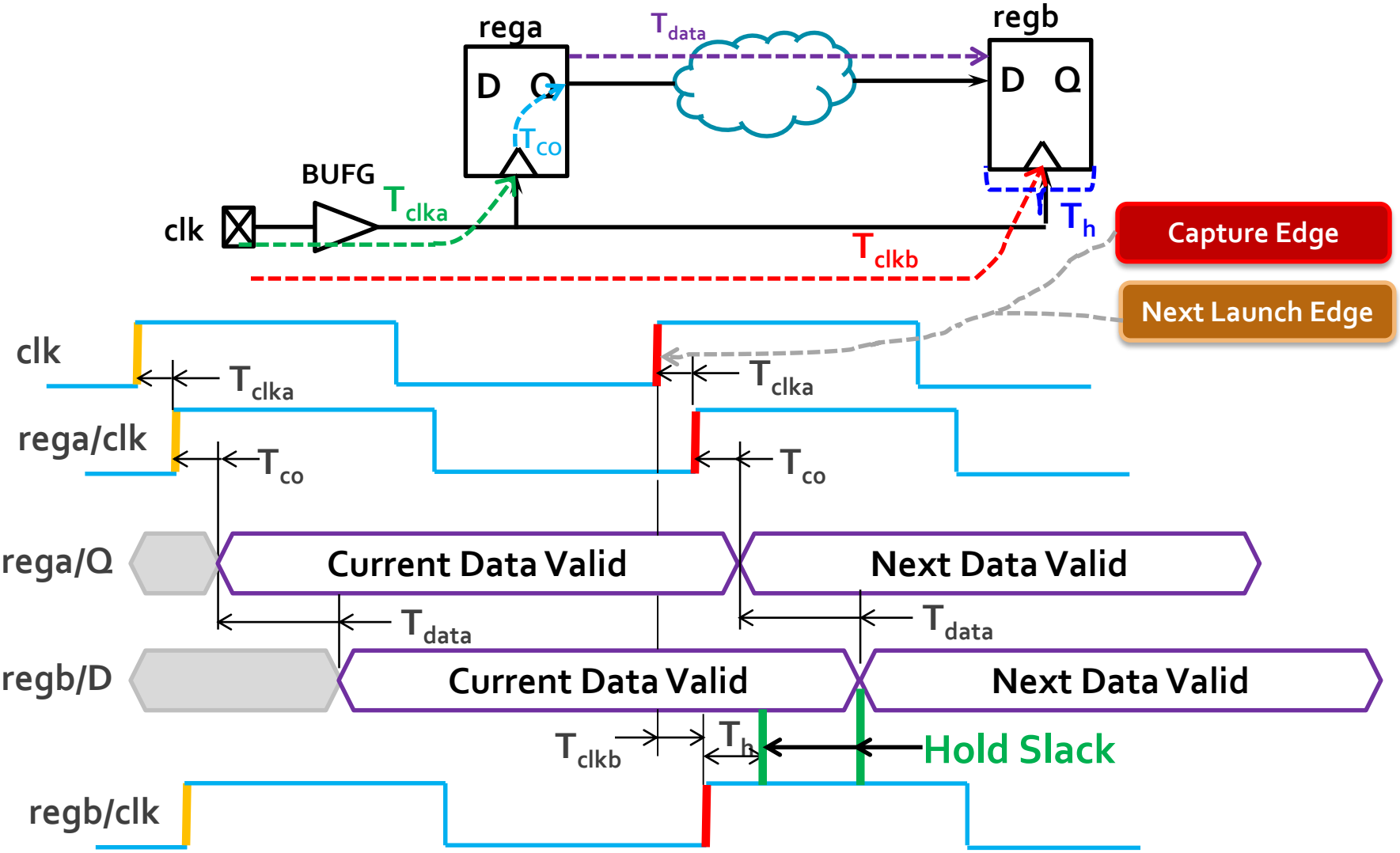
Setup Slack

The margin by which the setup timing requirement is met. It ensures launched data arrives in time to meet the capturing requirement



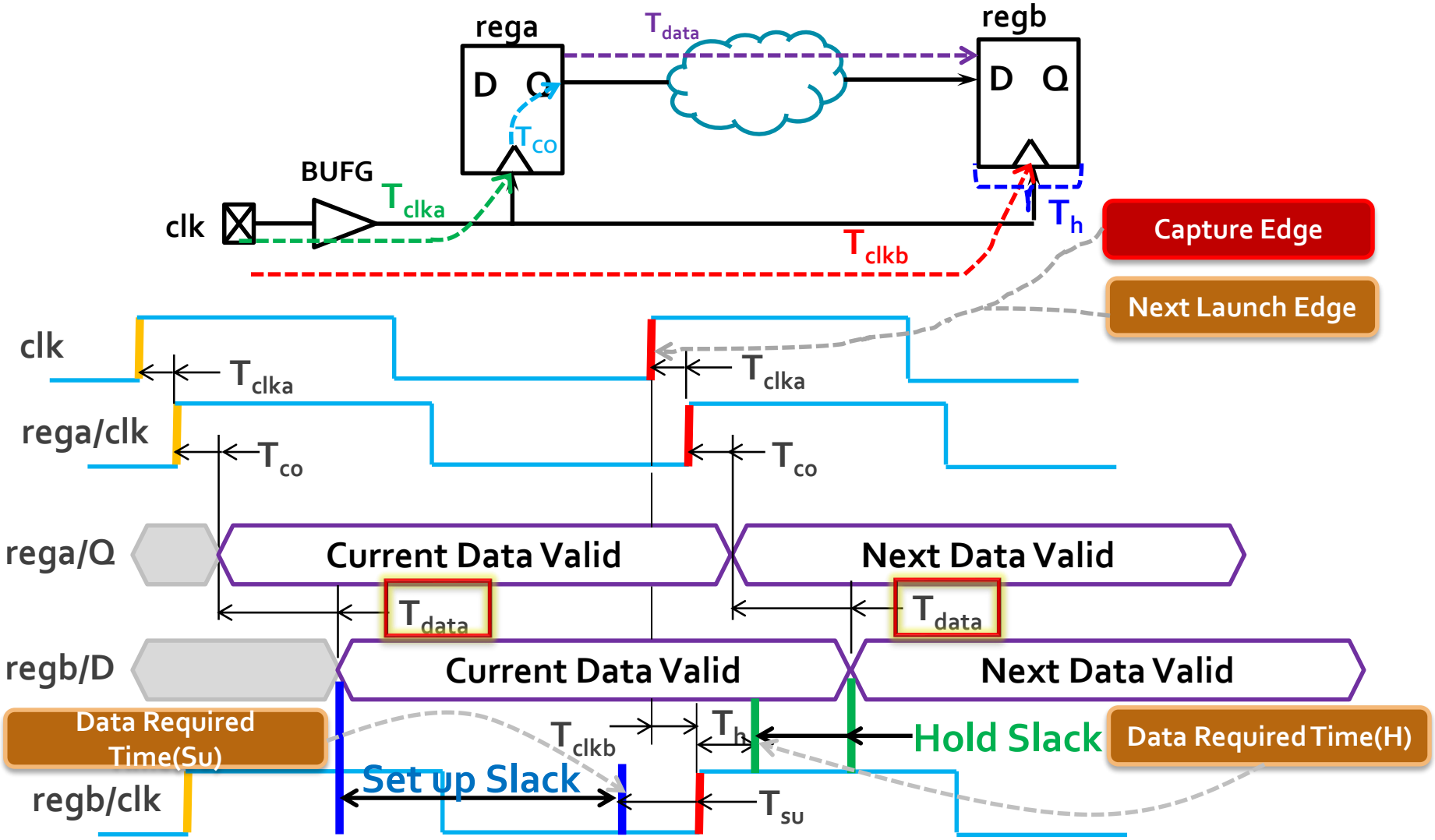
Hold Slack

The margin by which the hold timing requirement is met. It ensures capture data is not corrupted by data from another launch edge. It also prevents "double-clocking"



Setup & Hold Slack

The margin by which the hold timing requirement is met. It ensures capture data is not corrupted by data from another launch edge. It also prevents "double-clocking"



Slack Equations

Data Required Time (Setup) = Clock Arrival Time – T_{su} – Set up Uncertainty

Data Required Time (Hold) = Clock Arrival Time + Th + Hold Uncertainty

Setup Slack = Data Required Time (Setup) – Data Arrival Time (Setup)

Hold Slack = Data Arrival Time (Hold) – Data Required Time (Hold)

Positive slack: Timing requirement met

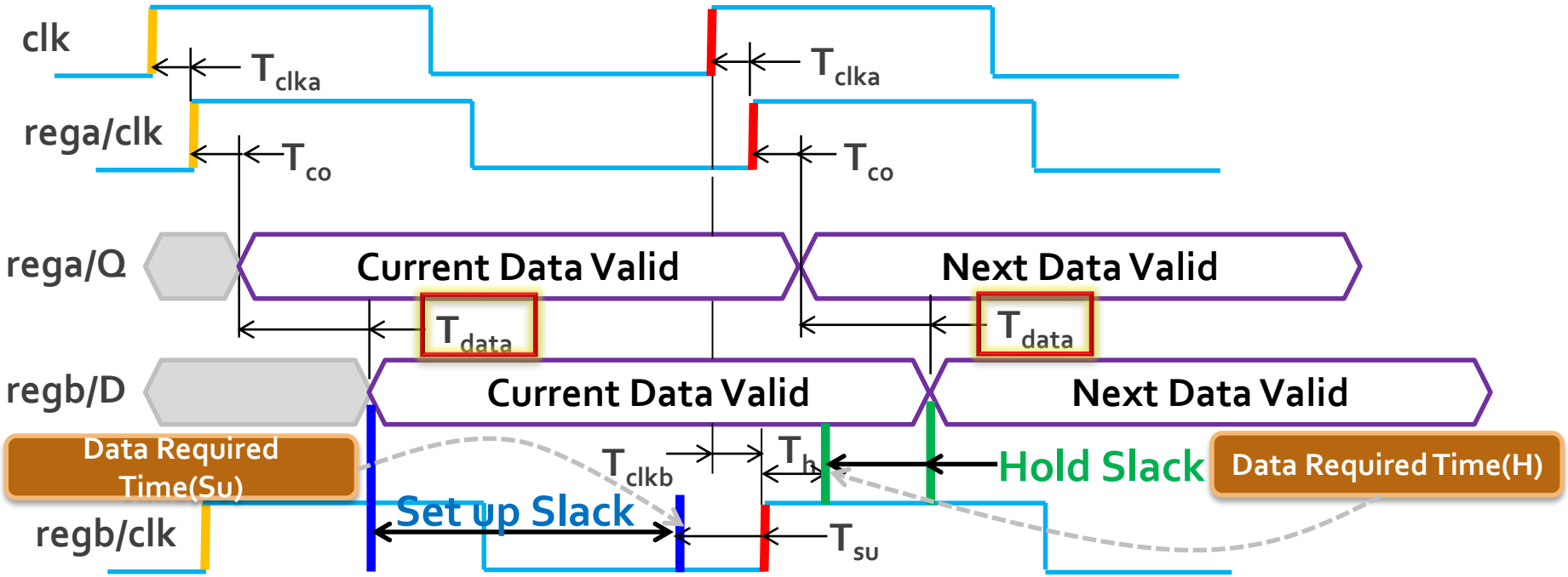
Negative slack: Timing requirement not met

Equations work for all timing path: Interal, I/O & asynchronous control

Why Is Slack Negative?

Setup Slack = Data Required Time (Setup) – Data Arrival Time (Setup)

Hold Slack = Data Arrival Time (Hold) – Data Required Time (Hold)



System Frequency

$$T_{data} = T_{\log ic} + T_{net}$$

$$T_s \geq T_{CO} + T_{data} + T_{su}$$

Summary

- Launch edge time is used as reference point during timing analysis
- Normally, capture edge time = launch edge time + 1 clock cycle
- T_{su} and T_h are dependent on the device which cannot be changed