Vivado从此开始（To Learn Vivado From Here）

本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用

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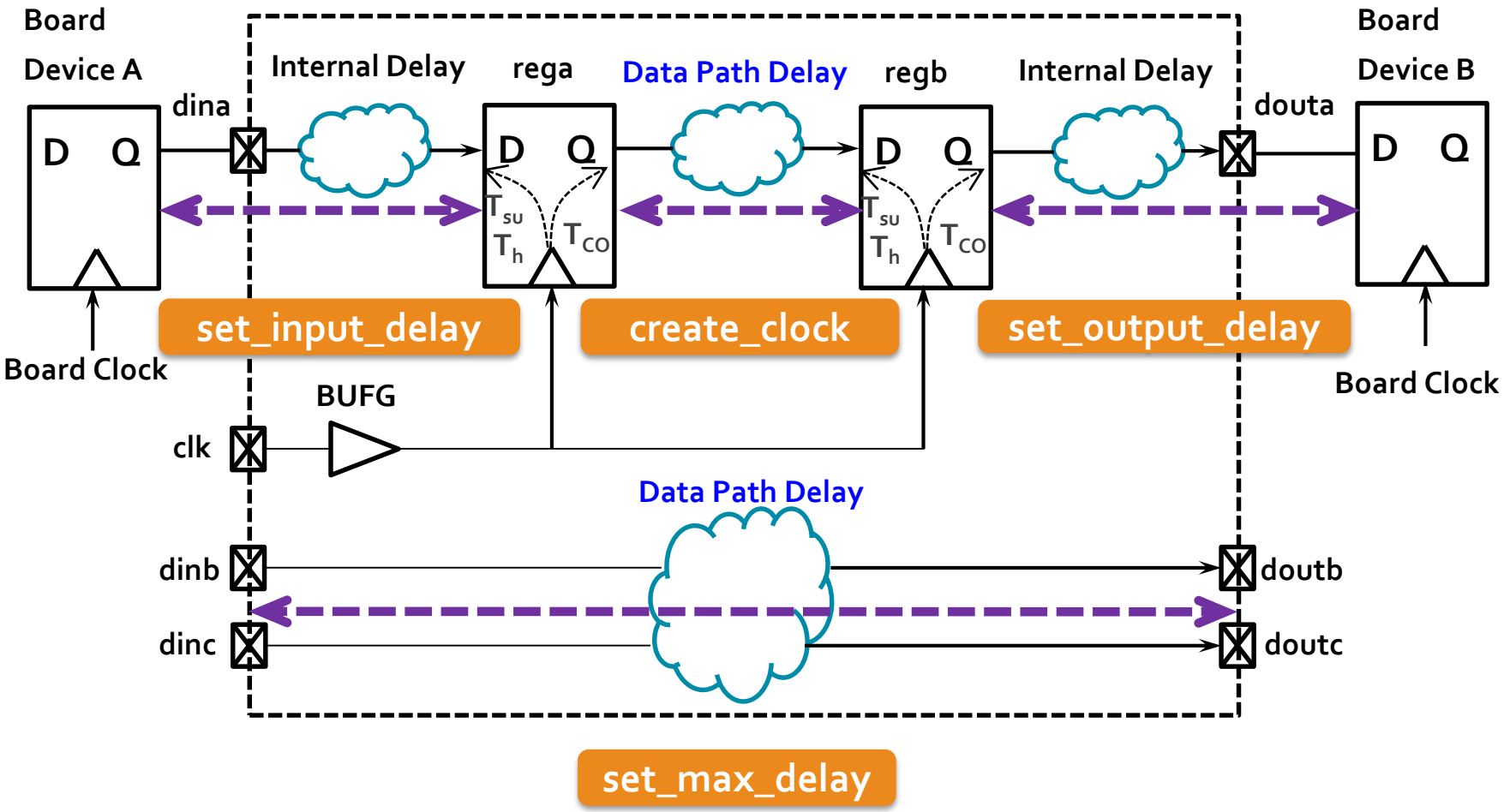
- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

- 内容翔实全面：涵盖Vivado所有基本功能
- 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- 描述图文并茂：给出具体操作步骤，易于快速动手实践

Setting Input Delay

Lauren Gao

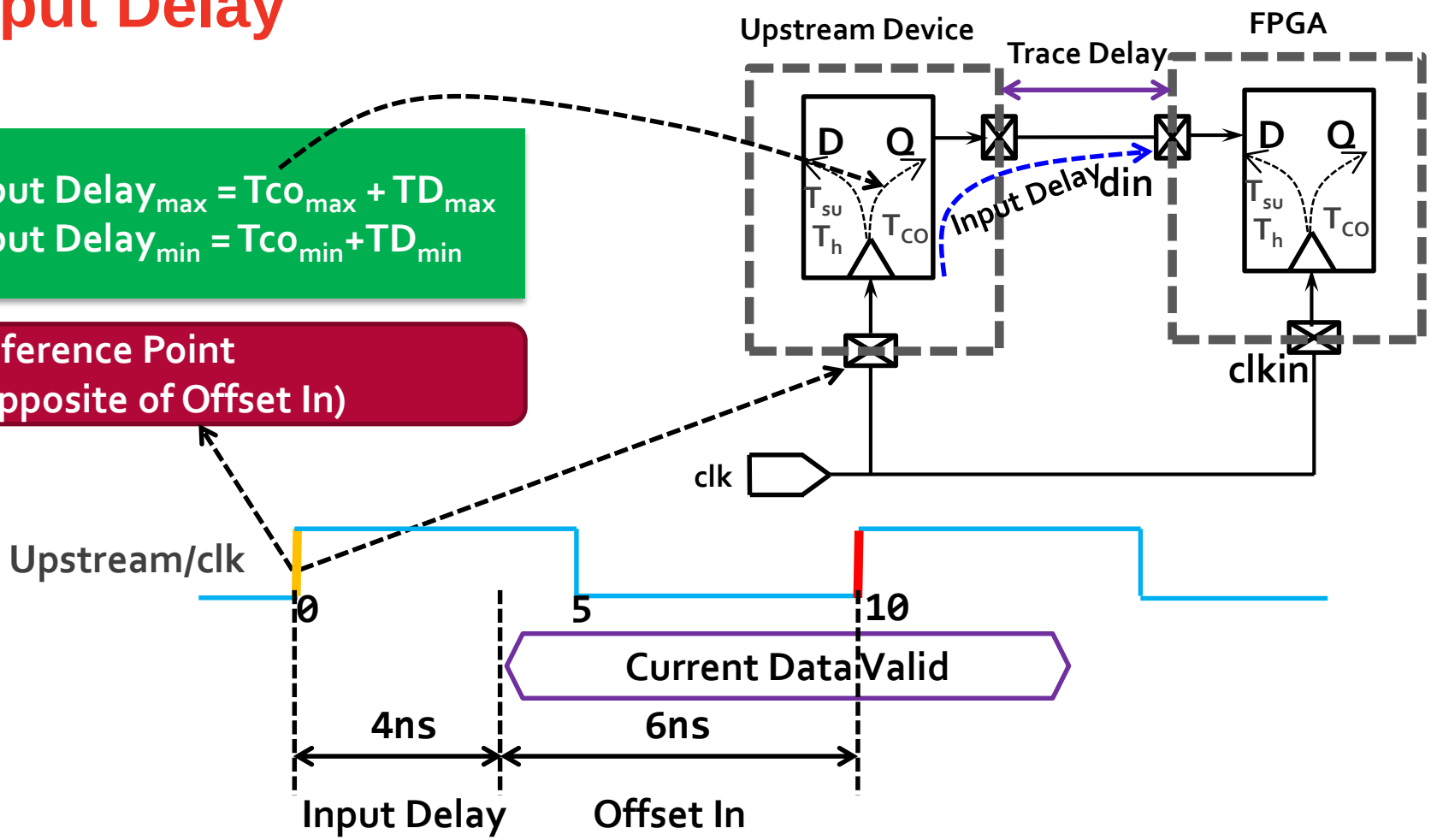
Different Paths Using Different Constraints



Input Delay

$\text{Input Delay}_{max} = \text{Tco}_{max} + \text{TD}_{max}$
$\text{Input Delay}_{min} = \text{Tco}_{min} + \text{TD}_{min}$

Reference Point
(Opposite of Offset In)



UCF

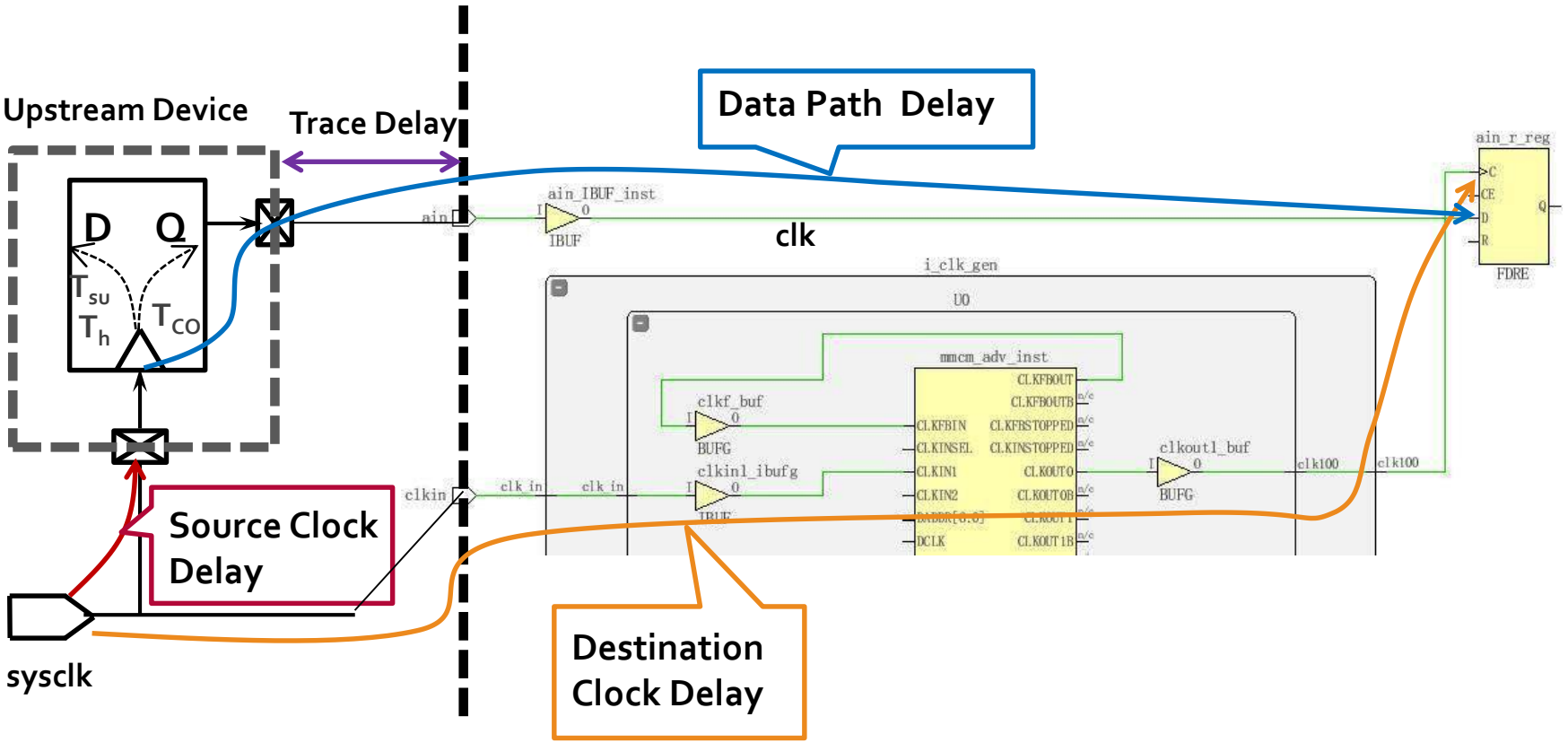
```
NET din OFFSET=IN 6ns BEFORE clkin
```

XDC

```
create_clock -name sysclk -period 10 [get_ports clkin]
set_input_delay -clock sysclk 4 [get_ports din]
```

Complete Input Static Timing Path

```
create_clock –name sysclk –period 10 [get_ports clkin]
set_input_delay -clock sysclk -max 4 [get_ports ain]
set_input_delay -clock sysclk -min 2 [get_ports ain]
```



Input Setup Timing Report Summary

```
Slack (MET) :             1.994ns  (required time - arrival time)
  Source:                 ain
                            (input port clocked by sysclk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:            ain_r_reg/D
                            (rising edge-triggered cell FDRE clocked by clk100_clk_gen_2  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             clk100_clk_gen_2
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (clk100_clk_gen_2 rise@10.000ns - sysclk rise@0.000ns)
  Data Path Delay:        1.745ns  (logic 0.986ns (56.477%)  route 0.760ns (43.523%))
  Logic Levels:           1  (IBUF=1)
  Input Delay:            4.000ns
  Clock Path Skew:        -2.022ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    -2.022ns = ( 7.978 - 10.000 )
    Source Clock Delay      (SCD):    0.000ns
    Clock Pessimism Removal (CPR):    0.000ns
  Clock Uncertainty:      0.172ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Discrete Jitter          (DJ):    0.129ns
    Phase Error              (PE):    0.099ns
```

Input Setup Timing Report Detailed Paths

```
Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
-------------------------------------------------------------------    -------------------
                     (clock sysclk rise edge)    0.000     0.000 r
                     input delay                 4.000     4.000
R10                                              0.000     4.000 r  ain
                     net (fo=0)                  0.000     4.000    ain
R10                  IBUF (Prop_ibuf_I_O)        0.986     4.986 r  ain_IBUF_inst/O
                     net (fo=1, routed)          0.760     5.745    ain_IBUF
SLICE_X0Y50          FDRE                                      r  ain_r_reg/D
-------------------------------------------------------------------    -------------------

                     (clock clk100_clk_gen_2 rise edge)
                                                10.000    10.000 r
N15                                              0.000    10.000 r  clkin
                     net (fo=0)                  0.000    10.000    i_clk_gen/U0/clk_in
N15                  IBUF (Prop_ibuf_I_O)        0.814    10.814 r  i_clk_gen/U0/clkin1_ibufg/O
                     net (fo=1, routed)          1.162    11.976    i_clk_gen/U0/clk_in_clk_gen
MMCME2_ADV_X0Y1      MMCME2_ADV (Prop_mmcme2_adv_CLKIN1_CLKOUT0)
                                                -7.322     4.654 r  i_clk_gen/U0/mmcm_adv_inst/CLKOUT0
                     net (fo=1, routed)          1.630     6.284    i_clk_gen/U0/clk100_clk_gen
BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)        0.091     6.375 r  i_clk_gen/U0/clkout1_buf/O
                     net (fo=3, routed)          1.603     7.978    clk100
SLICE_X0Y50                                                   r  ain_r_reg/C
                     clock pessimism             0.000     7.978
                     clock uncertainty          -0.172     7.806
SLICE_X0Y50          FDRE (Setup_fdre_C_D)      -0.067     7.739    ain_r_reg
-------------------------------------------------------------------

                     required time                         7.739
                     arrival time                         -5.745
-------------------------------------------------------------------
                     slack                                 1.994
```

Source Clock Delay

Data Path Delay

Destination Clock Delay

Slack Calculation

Input Hold Timing Report Summary

```
Slack (MET) :             3.143ns  (arrival time - required time)
  Source:                 ain
                            (input port clocked by sysclk {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:            ain_r_reg/D
                            (rising edge-triggered cell FDRE clocked by clk100_clk_gen_2 {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             clk100_clk_gen_2
  Path Type:              Hold (Min at Fast Process Corner)
  Requirement:            0.000ns  (clk100_clk_gen_2 rise@0.000ns - sysclk rise@0.000ns)
  Data Path Delay:        0.514ns  (logic 0.214ns (41.701%)  route 0.300ns (58.299%))
  Logic Levels:           1  (IBUF=1)
  Input Delay:            2.000ns
  Clock Path Skew:        -0.872ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    -0.872ns
    Source Clock Delay      (SCD):    0.000ns
    Clock Pessimism Removal (CPR):    -0.000ns
  Clock Uncertainty:      0.172ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Discrete Jitter          (DJ):    0.129ns
    Phase Error              (PE):    0.099ns
```

Input Hold Timing Report Detailed Paths

Location	Delay type	Incr(ns)	Path(ns)		Netlist Resource(s)
	(clock sysclk rise edge)	0.000	0.000	r	
	input delay	2.000	2.000		
R10		0.000	2.000	r	ain
	net (fo=0)	0.000	2.000		ain
R10	IBUF (Prop_ibuf_I_O)	0.214	2.214	r	ain_IBUF_inst/O
	net (fo=1, routed)	0.300	2.514		ain_IBUF
SLICE_X0Y50	FDRE			r	ain_r_reg/D
	(clock clk100_clk_gen_2 rise edge)				
		0.000	0.000	r	
N15		0.000	0.000	r	clkin
	net (fo=0)	0.000	0.000		i_clk_gen/U0/clk_in
N15	IBUF (Prop_ibuf_I_O)	0.365	0.365	r	i_clk_gen/U0/clkin1_ibufg/O
	net (fo=1, routed)	0.480	0.845		i_clk_gen/U0/clk_in_clk_gen
MMCME2_ADV_X0Y1	MMCME2_ADV (Prop_mmcme2_adv_CLKIN1_CLKOUT0)				
		-3.161	-2.316	r	i_clk_gen/U0/mmcm_adv_inst/CLKOUT0
	net (fo=1, routed)	0.540	-1.776		i_clk_gen/U0/clk100_clk_gen
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_O)	0.029	-1.747	r	i_clk_gen/U0/clkout1_buf/O
	net (fo=3, routed)	0.876	-0.872		clk100
SLICE_X0Y50				r	ain_r_reg/C
	clock pessimism	0.000	-0.872		
	clock uncertainty	0.172	-0.699		
SLICE_X0Y50	FDRE (Hold_fdre_C_D)	0.070	-0.629		ain_r_reg
	required time		0.629		
	arrival time		2.514		
	slack		3.143		

Source Clock Delay

Data Path Delay

Destination Clock Delay

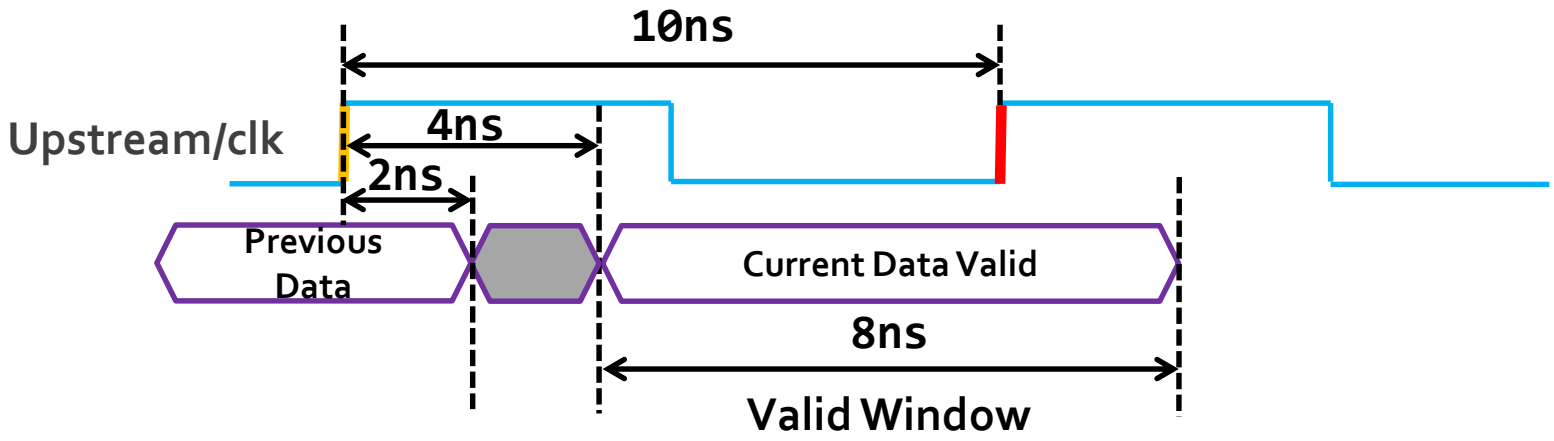
Slack Calculation

set_input_delay

set_input_delay [**-clock** *args*] [**-reference_pin** *args*] [**-clock_fall**] [**-rise**] [**-fall**] [**-max**] [**-min**] [**-add_delay**] [**-network_latency_included**] [**-source_latency_included**] [**-quiet**] [**-verbose**] *delay objects*

- **-clock**
  - Indicates that the input delay is relative to the specified clock. By default the **rising edg**e is used
  - However the **-clock_fall** argument can be used to indicate that the **falling edge** should be used instead
- **By default, each input port can have one maximum delay and one minimum delay**
  - Maximum delay is used for setup check
  - Minimum delay is used for hold check
- **Without the –max or –min option, the value supplied is used for both**

Input Setup and Hold XDC Examples



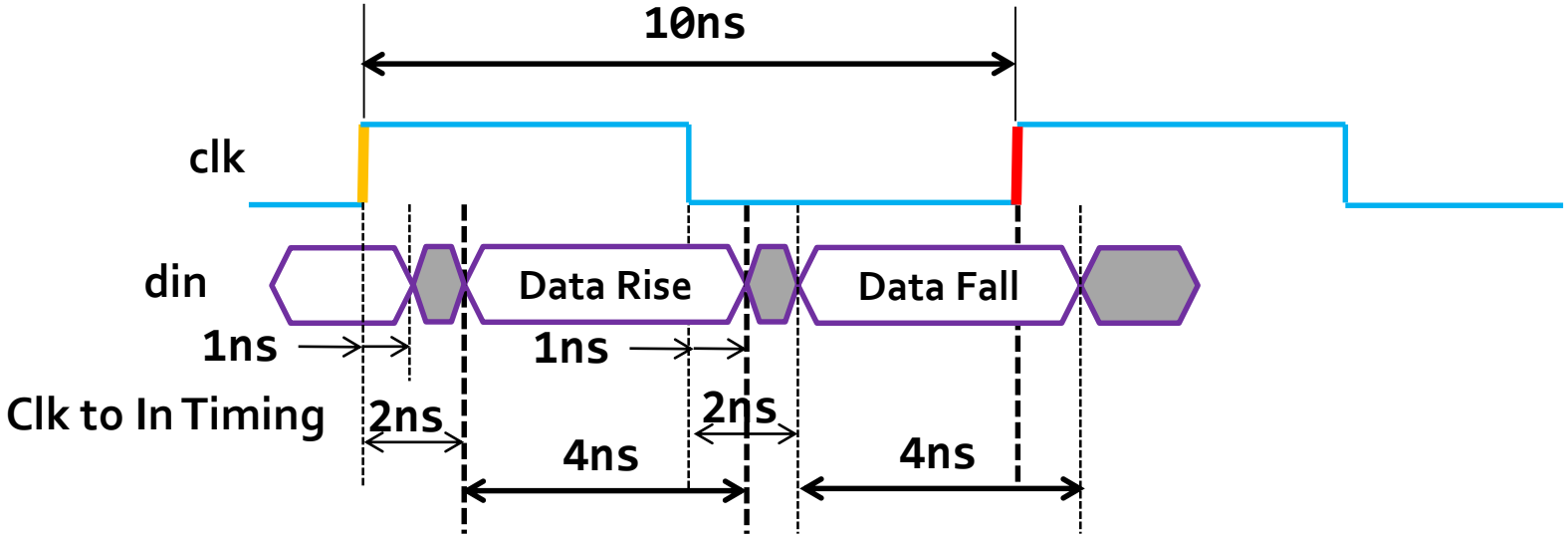
- max_delay is used for setup check calculation at the FPGA input

```
set_input_delay -clock sysclk -max 4 [get_ports din]
```

- min_delay is used for hold check calculation at the FPGA input

```
set_input_delay -clock sysclk -min 2 [get_ports din]
```

DDR Input Delay Example



- Use -clock_fall option to specify falling clock edge
- Us add_delay option needed to prevent falling edge max min constraints overriding existing max min delay constraints (for launch clock rising edge)

```
set_input_delay 1 –min –clock Clk [get_ports Data_In]
set_input_delay 2 –max –clock Clk [get_ports Data_In]
set_input_delay 1 –min –clock Clk [get_ports Data_In]\
-clock_fall –add_delay
set_input_delay 2 –max –clock Clk [get_ports Data_In]\
-clock_fall –add_delay
```

Static Timing Path

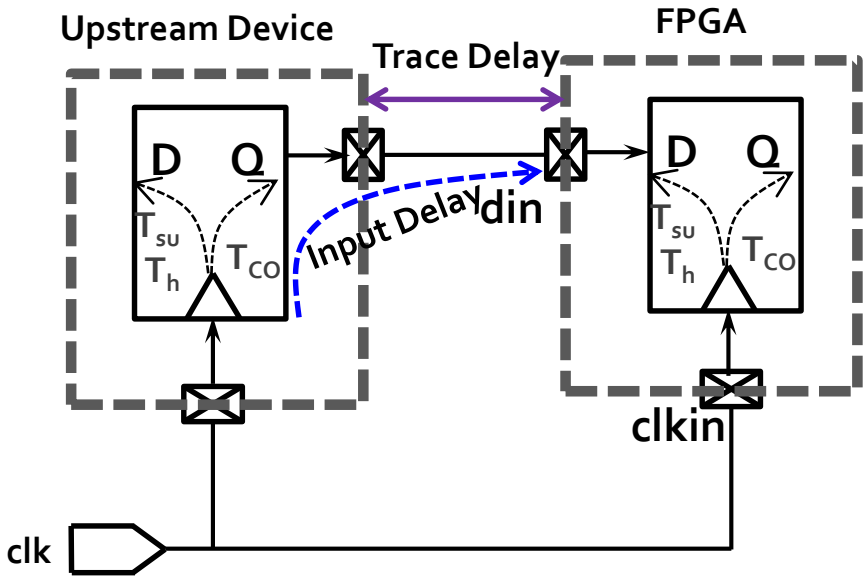
- **Static timing paths start at clocked elements and end at clocked elements**
  - Paths from internal flip-flop to internal flip-flop are constrained by clocks
  - Inputs and outputs of the FPGA are not startpoints/endpoints of static timing paths
- **By default, any logic between a primary I/O and an internal clocked element are not part of a complete static timing path**
  - Without additional commands, no setup/hold checks are done on logic associated with I/O

Complete the Static Timing Path

- To complete the static timing path we need to describe the external elements to the Vivado static timing engine
- Input port
  - What clock is used by the external device
  - The delay between the external device's clock and the arrival at the input port of the FPGA
    - Includes the CLK-Q time of the external device and the board delay
- Output port
  - The delay between output port of the FPGA and the external device's clock
    - Includes the required time of the external device and the board delay

Input Delay Summary

- Assume Tclk=10ns, Tco_{max}=2ns, TD_{max}=3ns, then we can constrain the input port as below
- This means the internal delay from din to FF/D in FPGA plus Tsu must be less than 10-2-3=5ns




```
set Tco_max 2.0
set TD_max 3.0
set Tco_min 0.0
set TD_min 0.0
create_clock -name sysclk -period 10 [get_ports clkin]
set_input_delay -clock sysclk -max [expr {$Tco_max+$TD_max}]\
[get_ports din]
set_input_delay -clock sysclk -min [expr {$Tco_min+$TD_min}]\
[get_ports din]
```