Vivado从此开始（To Learn Vivado From Here）

本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用

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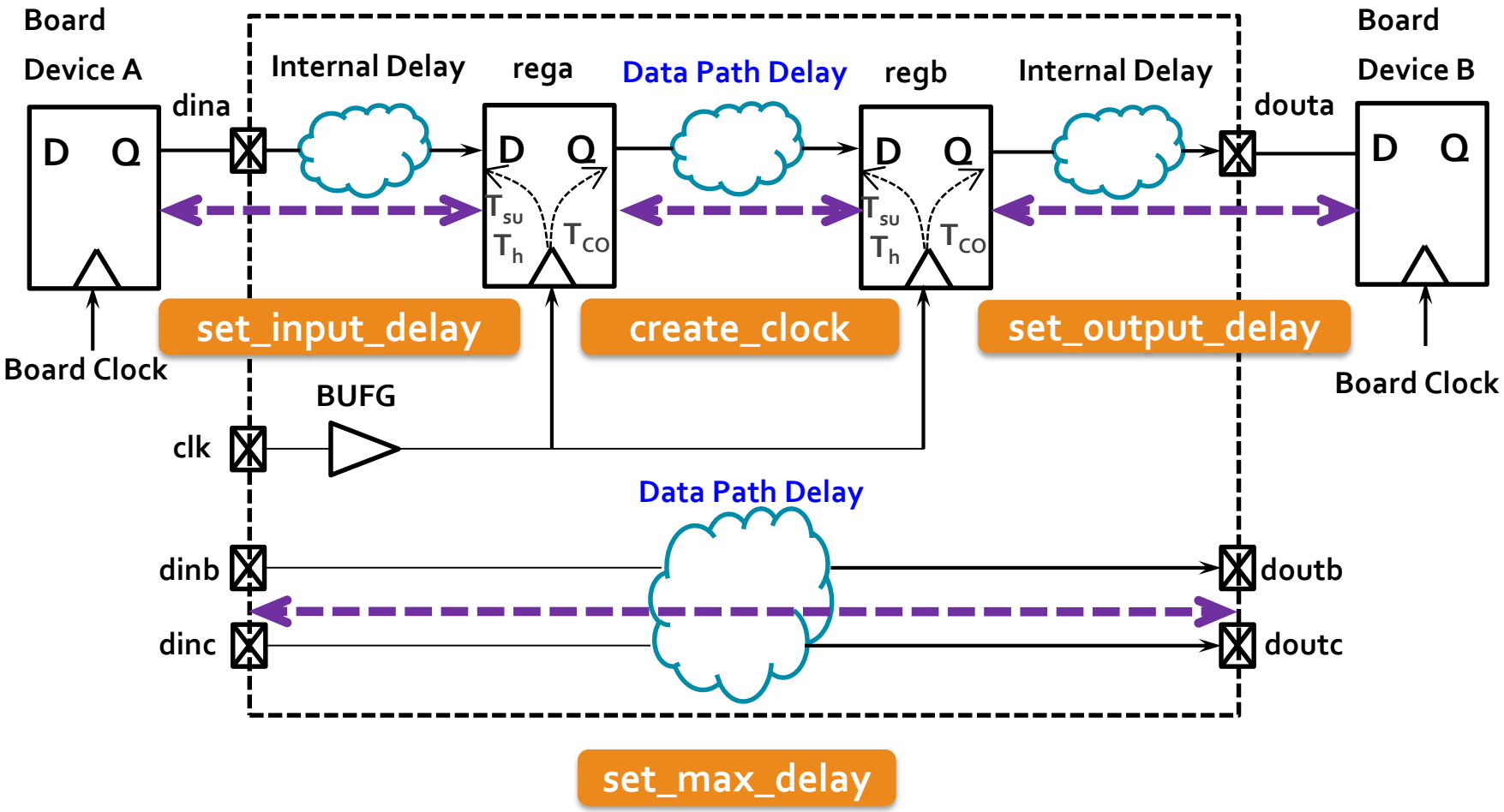
- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

- 内容翔实全面：涵盖Vivado所有基本功能
- 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- 描述图文并茂：给出具体操作步骤，易于快速动手实践

Setting Output Delay

Lauren Gao

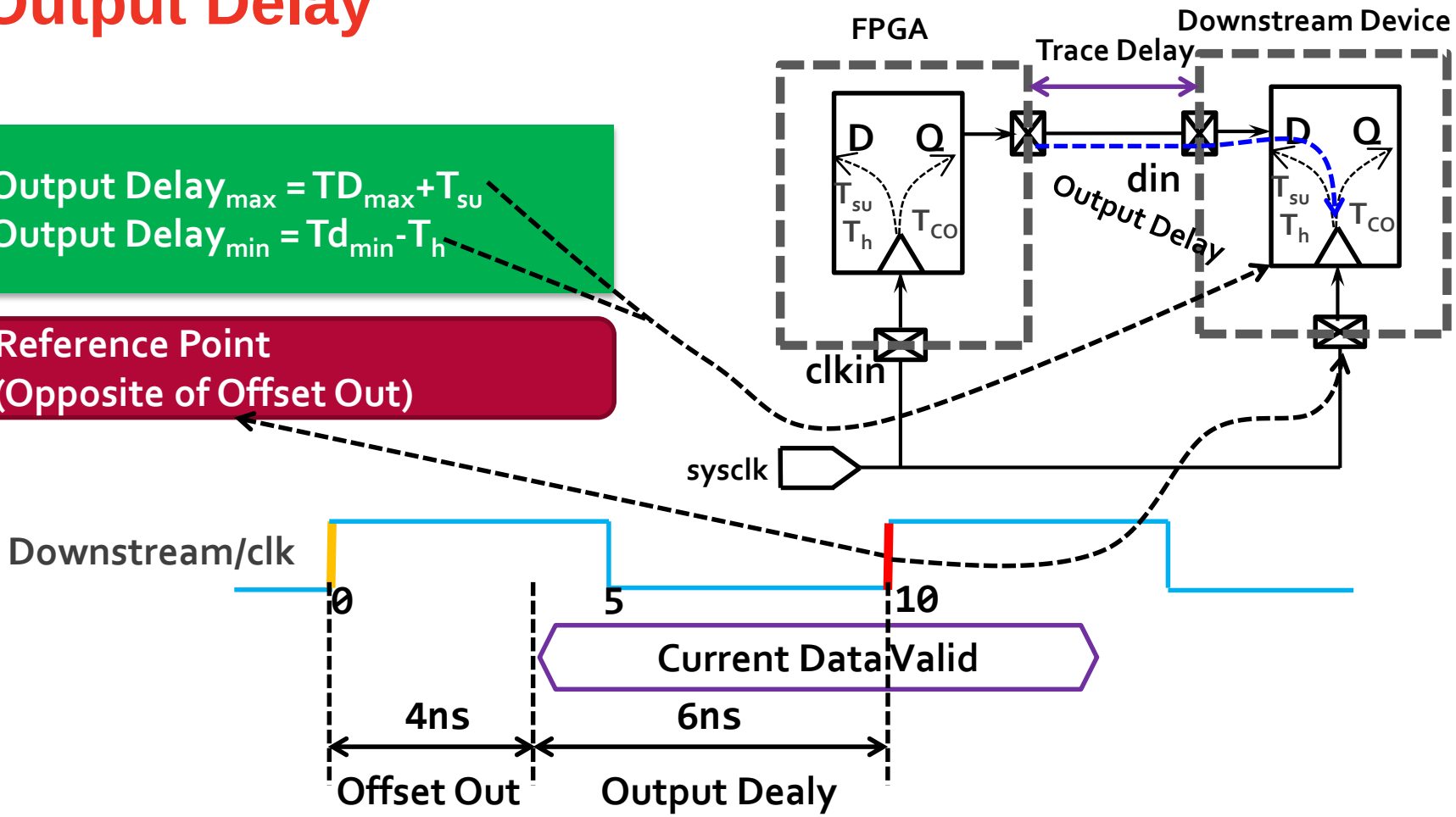
Different Paths Using Different Constraints



Output Delay

$Output\ Delay_{max} = TD_{max} + T_{su}$
$Output\ Delay_{min} = Td_{min} - T_h$

Reference Point
(Opposite of Offset Out)



UCF

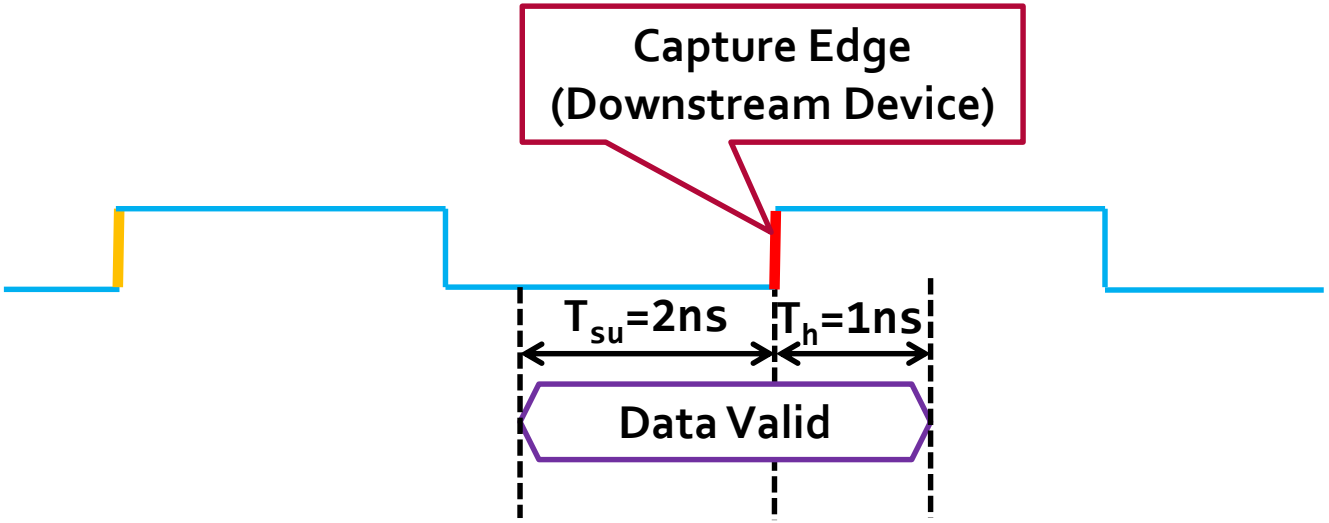
```
NET din OFFSET=OUT 4ns AFTER clkin
```

XDC

```
create_clock -name sysclk -period 10 [get_ports clkin]
set_output_delay -clock sysclk 6 [get_ports din]
```

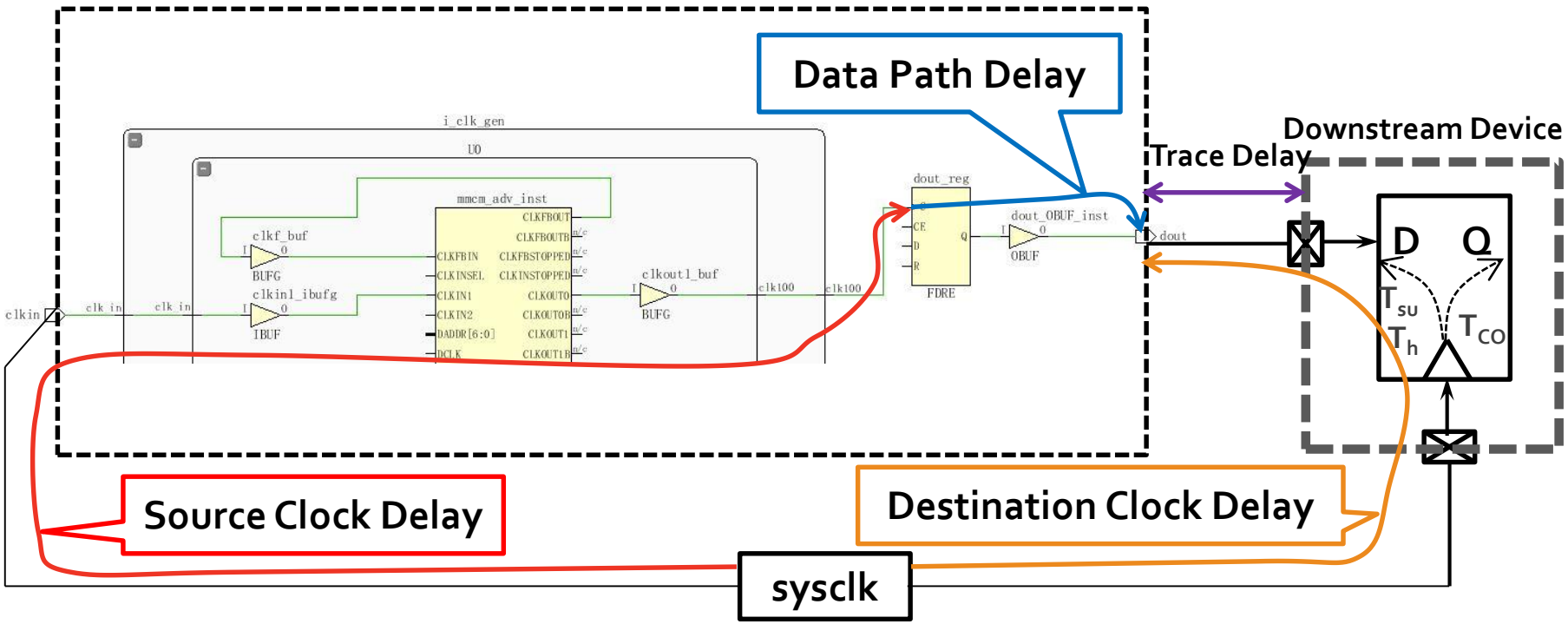
External Setup and Hold Requirements

- External devices need a setup and hold time around the clock
  - set_output_delay -max specifies the required setup time
  - set_output_delay -min specified the **negative** of the required hold time




```
create_clock –name sysclk –period 10 [get_ports clkin]
set_output_delay –clock sysclk –max 2 [get_ports dout]
set_output_delay –clock sysclk –min -1 [get_ports dout]
```

Complete Output Static Timing Path



- **Output static timing path is segmented slightly differently**
  - Data path delay ends at the port of the FPGA
  - Desgination clock path traces back through the downstream device to the port of the FPGA

Output Setup Timing Report Summary

```
Slack (MET) :             3.918ns  (required time - arrival time)
  Source:                 dout_reg/C
                            (rising edge-triggered cell FDRE clocked by clk100_clk_gen_2 {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:            dout
                            (output port clocked by sysclk {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             sysclk
  Path Type:              Max at Slow Process Corner
  Requirement:            10.000ns  (sysclk rise@10.000ns - clk100_clk_gen_2 rise@0.000ns)
  Data Path Delay:        5.267ns  (logic 3.123ns (59.301%)  route 2.144ns (40.699%))
  Logic Levels:           1  (OBUF=1)
  Output Delay:           2.000ns
  Clock Path Skew:        -1.357ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    0.000ns = ( 10.000 - 10.000 )
    Source Clock Delay      (SCD):    -1.357ns
    Clock Pessimism Removal (CPR):    0.000ns
  Clock Uncertainty:      0.172ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Discrete Jitter          (DJ):    0.129ns
    Phase Error              (PE):    0.099ns
```

Output Setup Timing Report Detailed Paths

```
  Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
-------------------------------------------------------------------    -------------------
                     (clock clk100_clk_gen_2 rise edge)
                                                0.000     0.000 r
N15                                             0.000     0.000 r     clkin
                     net (fo=0)                 0.000     0.000       i_clk_gen/U0/clk_in
N15                  IBUF (Prop_ibuf_I_O)       0.948     0.948 r     i_clk_gen/U0/clkin1_ibufg/O
                     net (fo=1, routed)         1.233     2.181       i_clk_gen/U0/clk_in_clk_gen
MMCME2_ADV_X0Y1      MMCME2_ADV (Prop_mmcme2_adv_CLKIN1_CLKOUT0)
                                               -7.069    -4.888 r     i_clk_gen/U0/mmcm_adv_inst/CLKOUT0
                     net (fo=1, routed)         1.710    -3.178       i_clk_gen/U0/clk100_clk_gen
BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)       0.096    -3.082 r     i_clk_gen/U0/clkout1_buf/O
                     net (fo=4, routed)         1.724    -1.357       clk100
SLICE_X0Y51                                                   r       dout_reg/C
-------------------------------------------------------------------    -------------------
SLICE_X0Y51          FDRE (Prop_fdre_C_Q)       0.456    -0.901 r     dout_reg/Q
                     net (fo=1, routed)         2.144     1.242       n_0_dout_reg
T9                   OBUF (Prop_obuf_I_O)       2.667     3.910 r     dout_OBUF_inst/O
                     net (fo=0)                 0.000     3.910       dout
T9                                                            r       dout
-------------------------------------------------------------------    -------------------

                     (clock sysclk rise edge)  10.000    10.000 r
                     clock pessimism            0.000    10.000
                     clock uncertainty         -0.172     9.828
                     output delay              -2.000     7.828
-------------------------------------------------------------------
                     required time                        7.828
                     arrival time                        -3.910
-------------------------------------------------------------------
                     slack                                3.918
```

Source Clock Delay

Data Path Delay

Destination Clock Delay

Slack Calculation

Output Hold Timing Report Summary

```
Slack (MET) :             0.052ns  (arrival time - required time)
  Source:                 dout_reg/C
                            (rising edge-triggered cell FDRE clocked by clk100_clk_gen_2 {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:            dout
                            (output port clocked by sysclk {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             sysclk
  Path Type:              Min at Fast Process Corner
  Requirement:            0.000ns  (sysclk rise@0.000ns - clk100_clk_gen_2 rise@0.000ns)
  Data Path Delay:        1.859ns  (logic 1.325ns (71.247%)  route 0.535ns (28.753%))
  Logic Levels:           1  (OBUF=1)
  Output Delay:           -1.000ns
  Clock Path Skew:        0.635ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    0.000ns
    Source Clock Delay      (SCD):    -0.635ns
    Clock Pessimism Removal (CPR):    -0.000ns
  Clock Uncertainty:      0.172ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Discrete Jitter          (DJ):    0.129ns
    Phase Error              (PE):    0.099ns
```

Output Hold Timing Report Detailed Paths

Location	Delay type	Incr(ns)	Path(ns)		Netlist Resource(s)
	(clock clk100_clk_gen_2 rise edge)				
		0.000	0.000	r	
N15		0.000	0.000	r	clkin
	net (fo=0)	0.000	0.000		i_clk_gen/U0/clk_in
N15	IBUF (Prop_ibuf_I_O)	0.177	0.177	r	i_clk_gen/U0/clkin1_ibufg/O
	net (fo=1, routed)	0.440	0.617		i_clk_gen/U0/clk_in_clk_gen
MMCME2_ADV_X0Y1	MMCME2_ADV (Prop_mmcme2_adv_CLKIN1_CLKOUT0)				
		-2.375	-1.759	r	i_clk_gen/U0/mmcm_adv_inst/CLKOUT0
	net (fo=1, routed)	0.495	-1.264		i_clk_gen/U0/clk100_clk_gen
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_O)	0.026	-1.238	r	i_clk_gen/U0/clkout1_buf/O
	net (fo=4, routed)	0.603	-0.635		clk100
SLICE_X0Y51				r	dout_reg/C
SLICE_X0Y51	FDRE (Prop_fdre_C_Q)	0.141	-0.494	r	dout_reg/Q
	net (fo=1, routed)	0.535	0.041		n_0_dout_reg
T9	OBUF (Prop_obuf_I_O)	1.184	1.224	r	dout_OBUF_inst/O
	net (fo=0)	0.000	1.224		dout
T9				r	dout
	(clock sysclk rise edge)	0.000	0.000	r	
	clock pessimism	0.000	0.000		
	clock uncertainty	0.172	0.172		
	output delay	1.000	1.172		
	required time		-1.172		
	arrival time		1.224		
	slack		0.052		

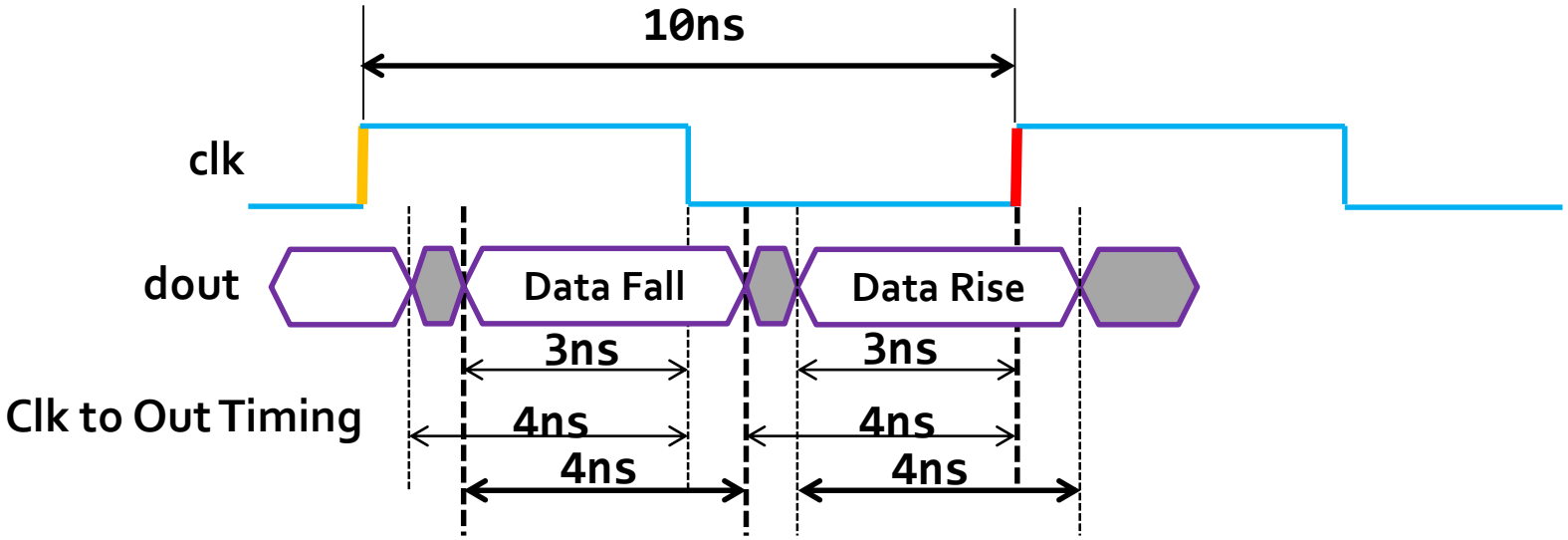
Source Clock Delay

Data Path Delay

Destination Clock Delay

Slack Calculation

System Synchronous DDR Output Delay Example



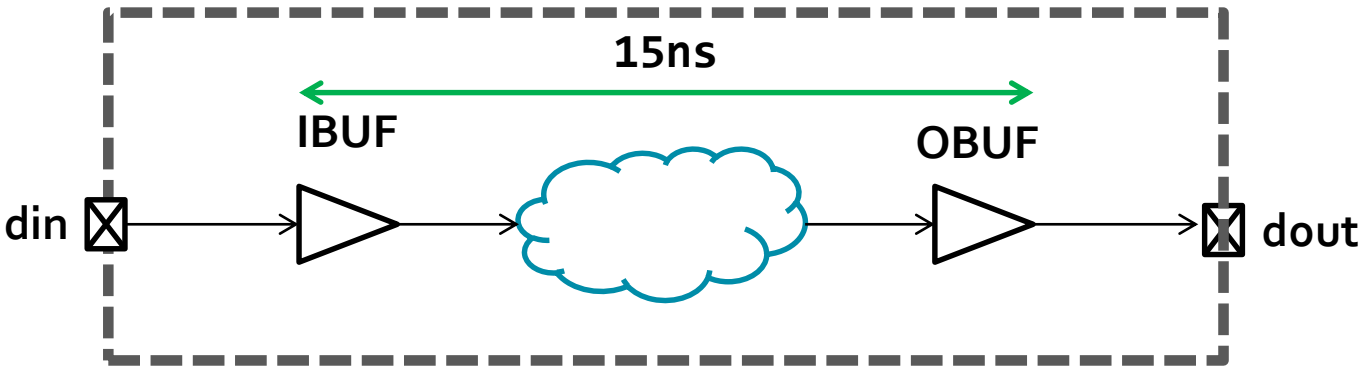

```
set_output_delay –min -1 –clock Clk [get_ports Data_Out]
set_output_delay –max  3 –clock Clk [get_ports Data_Out]
set_output_delay –min -1 –clock Clk [get_ports Data_Out]\
-clock_fall –add_delay
set_output_delay –max  3 –clock Clk [get_ports Data_Out]\
-clock_fall –add_delay
```

Output Delay Summary

- This depicts that the data must be ready at the output port before the required stable region starts and must remain stable until the end of the stable region
- This maps into a requirement on the timing of the logic to the output port inside the FPGA
- Use -clock_fall option to specify falling clock edge
- Use -add_delay option needed to prevent falling edge max min constraints overriding existing max min delay constraints (for rising edge)

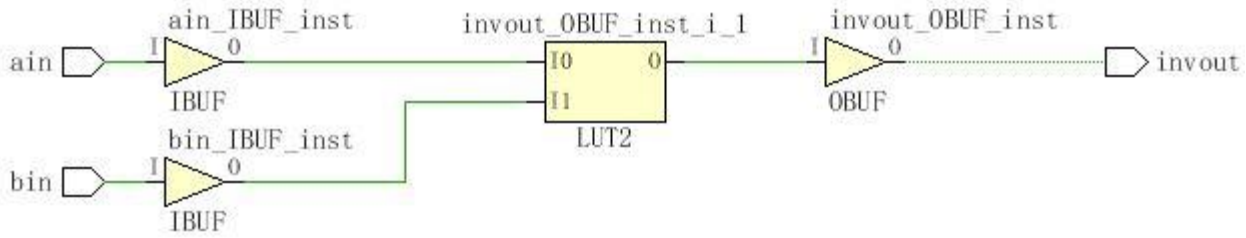
Asynchronous Input to Output Delay

- Use set_max_delay for combinational Input to Output delay




```
set_max_delay 15 –from [get_ports din] –to [get_ports dout]
```

set_max_delay Example




```
Slack (MET) :             7.525ns  (required time - arrival time)
  Source:                 ain
                            (input port)
  Destination:            invout
  Path Group:             **default**
  Path Type:              Max at Slow Process Corner
  Requirement:            15.000ns  (MaxDelay Path 15.000ns)
  Data Path Delay:        7.475ns  (logic 3.756ns (50.246%)  route 3.719ns (49.754%))
  Logic Levels:           3  (IBUF=1 LUT2=1 OBUF=1)
  Output Delay:           0.000ns
  Timing Exception:       MaxDelay Path 15.000ns
```

```
set_max_delay 15 -from [get_ports ain] -to [get_ports invout]
set_max_delay 15 -from [get_ports bin] -to [get_ports invout]
```

Timing Report of set_max_delay

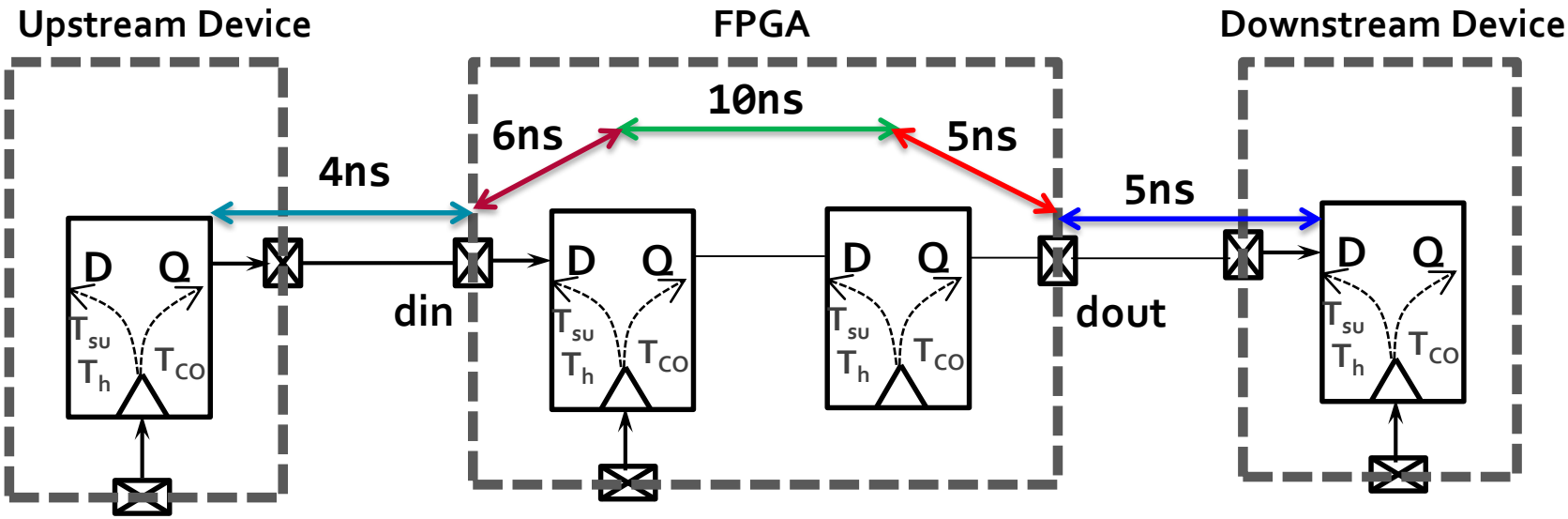
Location	Delay type	Incr(ns)	Path(ns)		Netlist Resource(s)
R10		0.000	0.000	r	ain
	net (fo=0)	0.000	0.000		ain
R10	IBUF (Prop_ibuf_I_O)	0.986	0.986	r	ain_IBUF_inst/O
	net (fo=2, routed)	1.358	2.343		ain_IBUF
SLICE_X0Y51	LUT2 (Prop_lut2_I0_O)	0.124	2.467	r	invout_OBUF_inst_i_1/O
	net (fo=1, routed)	2.361	4.829		n_0_invout_OBUF_inst_i_1
U13	OBUF (Prop_obuf_I_O)	2.646	7.475	r	invout_OBUF_inst/O
	net (fo=0)	0.000	7.475		invout
U13				r	invout
	max delay	15.000	15.000		
	clock pessimism	0.000	15.000		
	output delay	-0.000	15.000		
	required time		15.000		
	arrival time		-7.475		
	slack		7.525		

Data Path Delay

Path Delay Requirement

Slack Calculation

Example




```
create_clock –name sysclk –period 10 [get_ports clkin]
set_input_delay –clock sysclk 4 [get_ports din]
set_output_delay –clock sysclk 5 [get_ports dout]
```