Vivado从此开始（To Learn Vivado From Here）

本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用

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- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

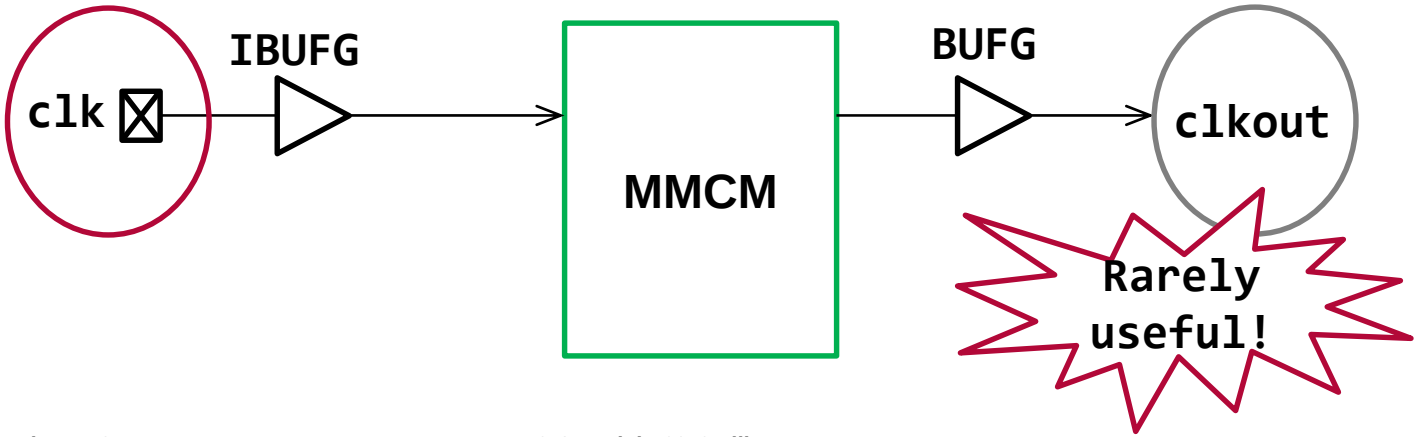
- 内容翔实全面：涵盖Vivado所有基本功能
- 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- 描述图文并茂：给出具体操作步骤，易于快速动手实践

Virtual Clock

Lauren Gao

Clocks for Input and Output Delay

- Clock specified by the set_input_delay and set_output_delay can be any clock from the clock database
  - Manually created clock attached to a clock input port of the FPGA
  - Derived clock generated inside the FPGA
    - This is legal, but rarely useful
- Sometimes the proper clock to use does not already exist
  - Virtual clocks can be created solely for the purpose of specifying input and output delays

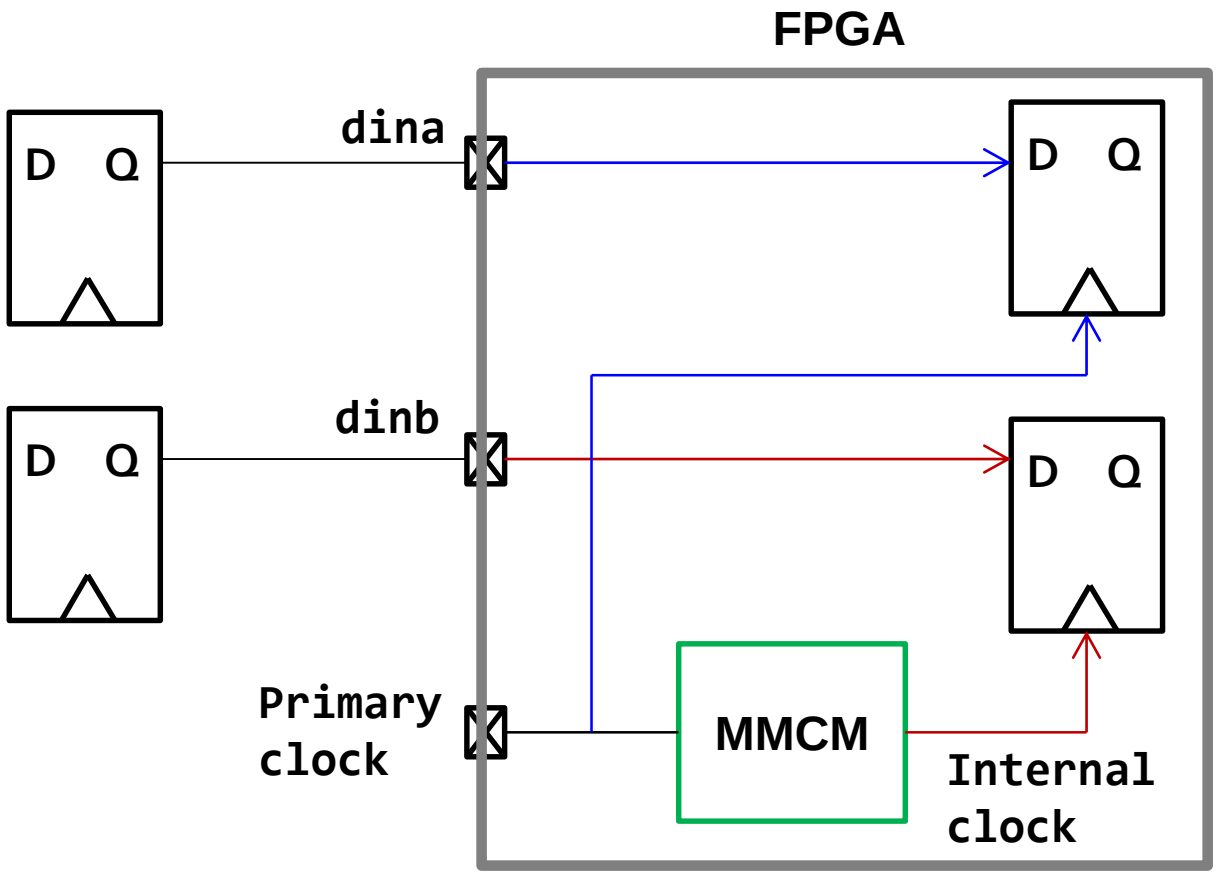


Reason for Using Virtual Clock

- There are many reasons for using virtual clocks for clocking I/O
  - Device external to the FPGA uses a different clock than the FPGA
    - Runs at a different frequency
      - Maybe a multiple/division of the FPGA clock
      - Maybe the frequency of an internal FPGA clock generated by an MMCM/PLL
    - Has a different delay path on the board
      - Maybe has clock buffer chip on the board
- XDC provides powerful mechanisms for describing clocks
  - Remember, all clocks in XDC are related by default

Primarily used to model system clocks for IO timing!

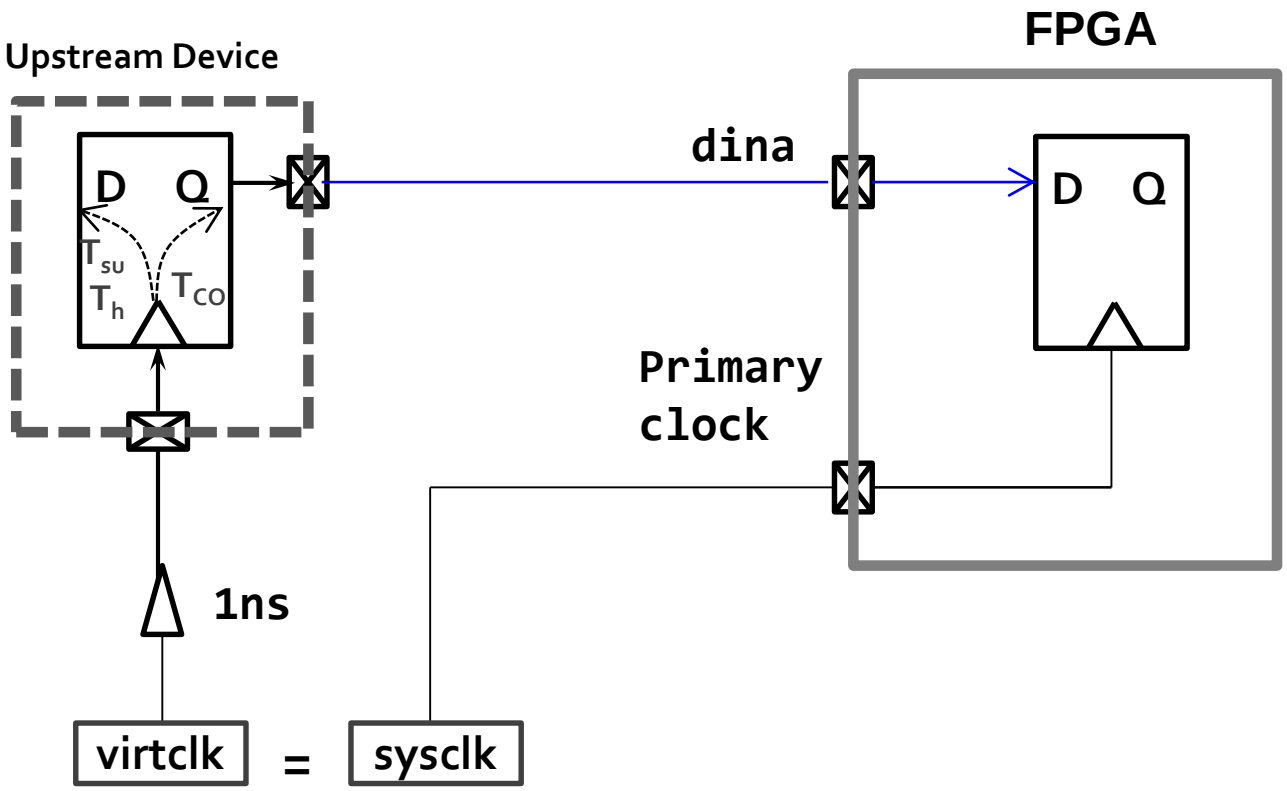
Virtual Clock for IO Timing – Example 1




```
create_clock -name sysclk -period 10 [get_ports clkin]
create_clock -name vclk -period 5
set_input_delay 6 –clock clk [get_ports dina]
Set_input_delay 6 –clock vclk [get_ports dinb]
```

Vclk has same period as internal clock (MMCM output clock)!

Virtual Clock for IO Timing – Example 2



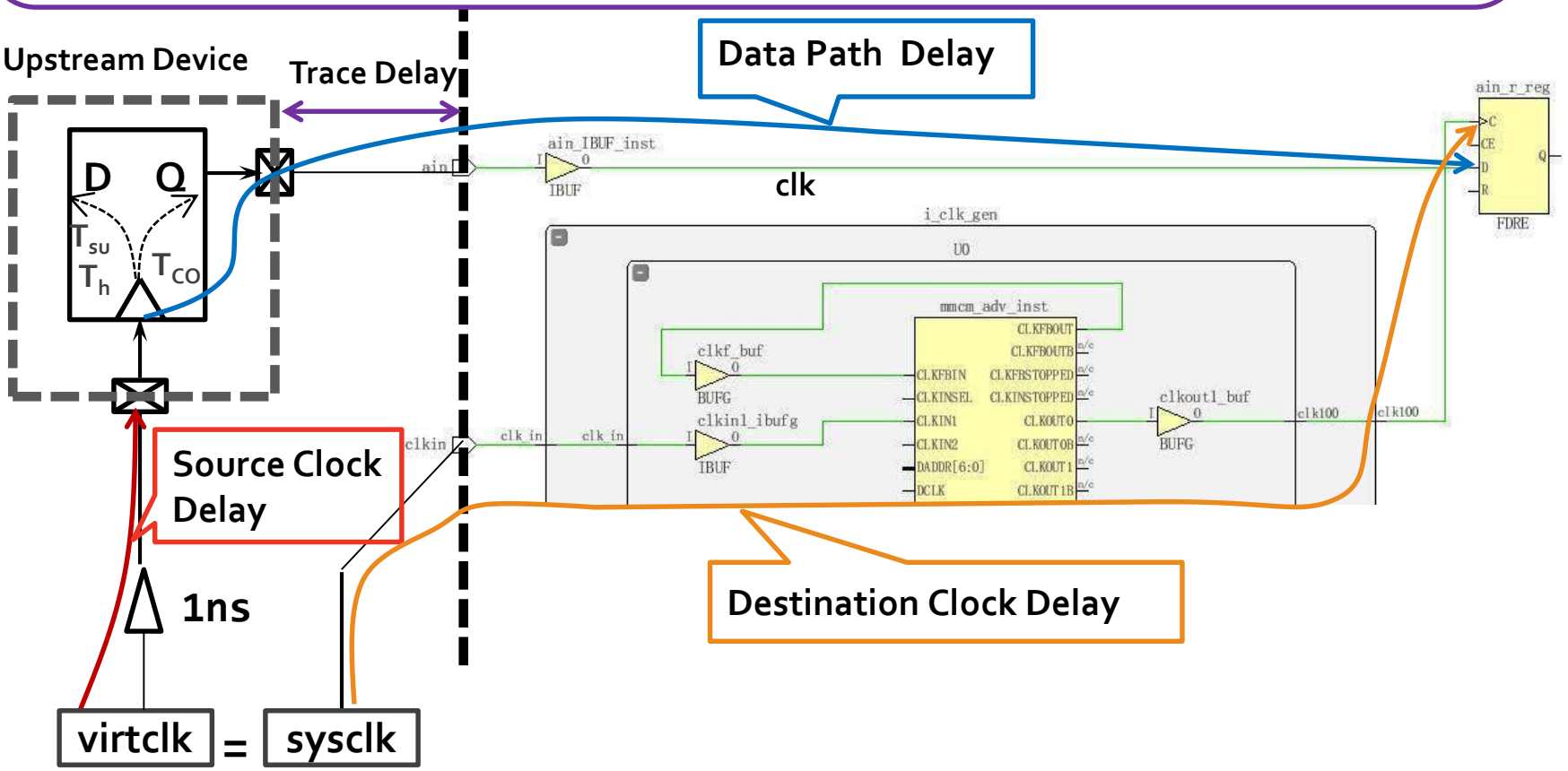

```
create_clock -name sysclk -period 10 [get_ports clkin]
create_clock -name virtclk -period 10
set_clock_latency -source 1 [get_clocks virtclk]
set_input_delay -clock virtclk -max 4 [get_ports ain]
set_input_delay -clock virtclk -min 2 [get_ports ain]
```

Creating Virtual Clocks

- **Virtual clocks are created with create_clock**
  - Create clock is not attached to any design objects
  - create_clock -name <name> -period <period>
    - <period> is the period of the clock
    - <name> is the user assigned name for the clock
    - Can use the -waveform option
- **Can specify jitter with the set_input_jitter command**
- **Can set clock latency with the set_clock_latency -source command**
- **Virtual clocks are placed in the design database and can be accessed like other clocks**
  - Can be seen via the report_clocks command
  - Can be accessed by the get_clocks command

Input Static Timing Path with External Buffer

```
create_clock -name sysclk -period 10 [get_ports clkin]
create_clock -name virtclk -period 10
set_clock_latency -source 1 [get_clocks virtclk]
set_input_delay -clock virtclk -max 4 [get_ports ain]
set_input_delay -clock virtclk -min 2 [get_ports ain]
```



Report Clock for Virtual Clock

```
Attributes
  P: Propagated
  G: Generated
  V: Virtual
  I: Inverted

Clock                Period    Waveform           Attributes  Sources
sysclk               10.00000  {0.00000 5.00000}  P           {clkin}
virtclk              10.00000  {0.00000 5.00000}  V           {}
clkfbout_clk_gen_2   10.00000  {0.00000 5.00000}  P,G         {i_clk_gen/U0/mmcm_adv_inst/CLKFBOUT}
clk100_clk_gen_2     10.00000  {0.00000 5.00000}  P,G         {i_clk_gen/U0/mmcm_adv_inst/CLKOUT0}


====================================================
Generated Clocks
====================================================

Generated Clock    : clkfbout_clk_gen_2
Master Source      : i_clk_gen/U0/mmcm_adv_inst/CLKIN1
Master Clock       : sysclk
Multiply By        : 1
Generated Sources  : {i_clk_gen/U0/mmcm_adv_inst/CLKFBOUT}

Generated Clock    : clk100_clk_gen_2
Master Source      : i_clk_gen/U0/mmcm_adv_inst/CLKIN1
Master Clock       : sysclk
Multiply By        : 1
Generated Sources  : {i_clk_gen/U0/mmcm_adv_inst/CLKOUT0}
```

Input Setup Timing Report Summary with Virtual Clock

```
Slack (MET) :             0.998ns  (required time - arrival time)
  Source:                 ai
                            (input port clocked by virtclk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:            a
                            (rising edge-triggered cell FDRE clocked by clk100_clk_gen_2  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             clk100_clk_gen_2
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (clk100_clk_gen_2 rise@10.000ns - virtclk rise@0.000ns)
  Data Path Delay:        1.745ns  (logic 0.986ns (56.477%)  route 0.760ns (43.523%))
  Logic Levels:           1  (IBUF=1)
  Input Delay:            4.000ns
  Clock Path Skew:        -3.022ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    -2.022ns = ( 7.978 - 10.000 )
    Source Clock Delay      (SCD):    1.000ns
    Clock Pessimism Removal (CPR):    0.000ns
  Clock Uncertainty:      0.168ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter     (TSJ):    0.050ns
    Discrete Jitter          (DJ):    0.129ns
    Phase Error              (PE):    0.099ns
```

Input Setup Timing Report Detailed Paths with Virtual Clock

```
Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
-------------------------------------------------------------------  -------------------
                     (clock virtclk rise edge)    0.000     0.000 r
                     clock source latency         1.000     1.000
                     ideal clock network latency
                                                  0.000     1.000
                     input delay                  4.000     5.000
R10                                               0.000     5.000 r  ain
                     net (fo=0)                   0.000     5.000    ain
R10                  IBUF (Prop_ibuf_I_O)         0.986     5.986 r  ain_IBUF_inst/O
                     net (fo=1, routed)           0.760     6.745    ain_IBUF
SLICE_X0Y50          FDRE                                        r  ain_r_reg/D
-------------------------------------------------------------------  -------------------

                     (clock clk100_clk_gen_2 rise edge)
                                                 10.000    10.000 r
N15                                               0.000    10.000 r  clkin
                     net (fo=0)                   0.000    10.000    i_clk_gen/U0/clk_in
N15                  IBUF (Prop_ibuf_I_O)         0.814    10.814 r  i_clk_gen/U0/clkin1_ibufg/O
                     net (fo=1, routed)           1.162    11.976    i_clk_gen/U0/clk_in_clk_gen
MMCME2_ADV_X0Y1      MMCME2_ADV (Prop_mmcme2_adv_CLKIN1_CLKOUT0)
                                                 -7.322     4.654 r  i_clk_gen/U0/mmcm_adv_inst/CLKOUT0
                     net (fo=1, routed)           1.630     6.284    i_clk_gen/U0/clk100_clk_gen
BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.091     6.375 r  i_clk_gen/U0/clkout1_buf/O
                     net (fo=4, routed)           1.603     7.978    clk100
SLICE_X0Y50                                                     r  ain_r_reg/C
                     clock pessimism              0.000     7.978
                     clock uncertainty           -0.168     7.810
SLICE_X0Y50          FDRE (Setup_fdre_C_D)       -0.067     7.743    ain_r_reg
-------------------------------------------------------------------

                     required time                          7.743
                     arrival time                          -6.745
-------------------------------------------------------------------
                     slack                                  0.998
```

Source Clock Delay

Data Path Delay

Destination Clock Delay

Slack Calculation

Input Hold Timing Report Summary with Virtual Clock

```
Slack (MET) :             4.148ns  (arrival time - required time)
  Source:                 ai
                            (input port clocked by virtclk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:            ai
                            (rising edge-triggered cell FDRE clocked by clk100_clk_gen_2  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             clk100_clk_gen_2
  Path Type:              Hold (Min at Fast Process Corner)
  Requirement:            0.000ns  (clk100_clk_gen_2 rise@0.000ns - virtclk rise@0.000ns)
  Data Path Delay:        0.514ns  (logic 0.214ns (41.701%)  route 0.300ns (58.299%))
  Logic Levels:           1  (IBUF=1)
  Input Delay:            2.000ns
  Clock Path Skew:        -1.872ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    -0.872ns
    Source Clock Delay      (SCD):    1.000ns
    Clock Pessimism Removal (CPR):    -0.000ns
  Clock Uncertainty:      0.168ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter     (TSJ):    0.050ns
    Discrete Jitter          (DJ):    0.129ns
    Phase Error              (PE):    0.099ns
```

Input Hold Timing Report Detailed Paths with Virtual Clock

Location	Delay type	Incr(ns)	Path(ns)		Netlist Resource(s)
	(clock virtclk rise edge)	0.000	0.000	r	
	clock source latency	1.000	1.000		
	ideal clock network latency				
		0.000	1.000		
	input delay	2.000	3.000		
R10		0.000	3.000	r	ain
	net (fo=0)	0.000	3.000		ain
R10	IBUF (Prop_ibuf_I_O)	0.214	3.214	r	ain_IBUF_inst/O
	net (fo=1, routed)	0.300	3.514		ain_IBUF
SLICE_X0Y50	FDRE			r	ain_r_reg/D
	(clock clk100_clk_gen_2 rise edge)				
		0.000	0.000	r	
N15		0.000	0.000	r	clkin
	net (fo=0)	0.000	0.000		i_clk_gen/U0/clk_in
N15	IBUF (Prop_ibuf_I_O)	0.365	0.365	r	i_clk_gen/U0/clkin1_ibufg/O
	net (fo=1, routed)	0.480	0.845		i_clk_gen/U0/clk_in_clk_gen
MMCME2_ADV_X0Y1	MMCME2_ADV (Prop_mmcme2_adv_CLKIN1_CLKOUT0)				
		-3.161	-2.316	r	i_clk_gen/U0/mmcm_adv_inst/CLKOUT0
	net (fo=1, routed)	0.540	-1.776		i_clk_gen/U0/clk100_clk_gen
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_O)	0.029	-1.747	r	i_clk_gen/U0/clkout1_buf/O
	net (fo=4, routed)	0.876	-0.872		clk100
SLICE_X0Y50				r	ain_r_reg/C
	clock pessimism	0.000	-0.872		
	clock uncertainty	0.168	-0.704		
SLICE_X0Y50	FDRE (Hold_fdre_C_D)	0.070	-0.634		ain_r_reg
	required time		0.634		
	arrival time		3.514		
	slack		4.148		

Source Clock Delay

Data Path Delay

Destination Clock Delay

Slack Calculation

Complete the Static Timing Path

- To complete the static timing path we need to describe the external elements to the Vivado static timing engine
- Input port
  - What clock is used by the external device
  - The delay between the external device's clock and the arrival at the input port of the FPGA
    - Includes the CLK-Q time of the external device and the board delay
- Output port
  - The delay between output port of the FPGA and the external device's clock
    - Includes the required time of the external device and the board delay