Vivado从此开始（To Learn Vivado From Here）

本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用

作者：高亚军（Xilinx战略应用高级工程师）

- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

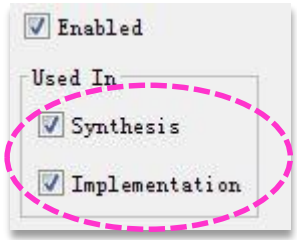
- 内容翔实全面：涵盖Vivado所有基本功能
- 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- 描述图文并茂：给出具体操作步骤，易于快速动手实践

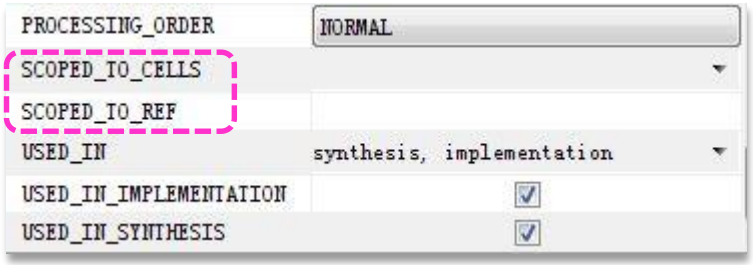
XDC Precedence

Lauren Gao

Organizing the Design Constraints

- **Recommended constraint files**
  - Simple design





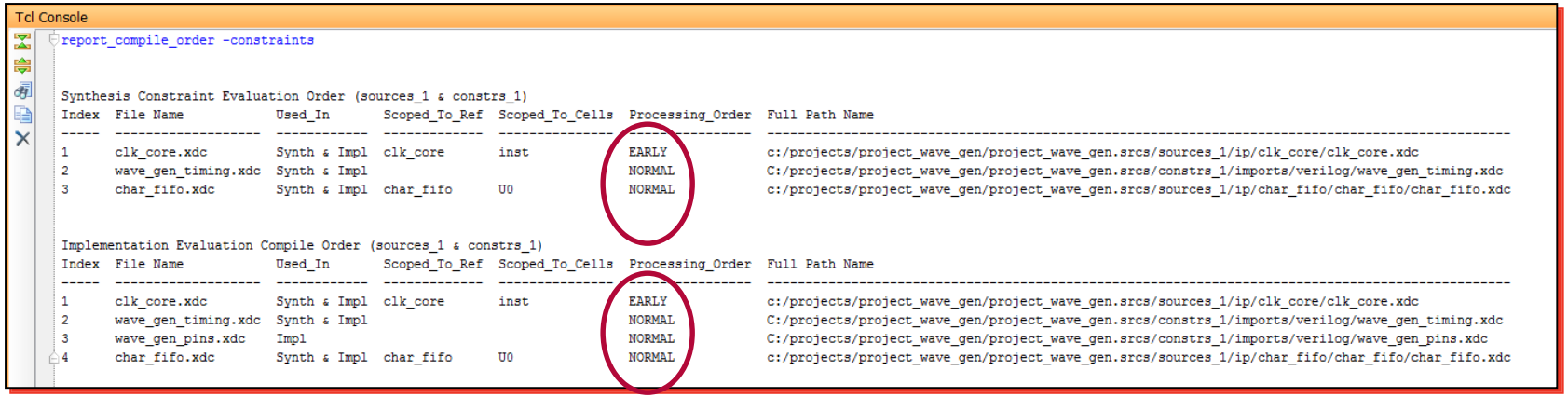
1. All
2. Phy + Timing
3. Phy + Timing (Synth) + Timing (Impl)

  - Complex design

Top-level Timing + Top-level Phy + IP

Include IP Constraints

- **Many cores have their own constraints / exceptions**
  - PCIE, MIG, RAM-based asynchronous FIFOs…
- **Non-native IP: Be careful!**
  - Very easy to drop the IP constraints especially if provided as .ngc files
- **Native IP: Constraints included**
  - Sources window in IDE: Compile Order → Constraints
  - Use **`report_compile_order -constraints`** to identify constraint file sources



Managing IP Constraint Files

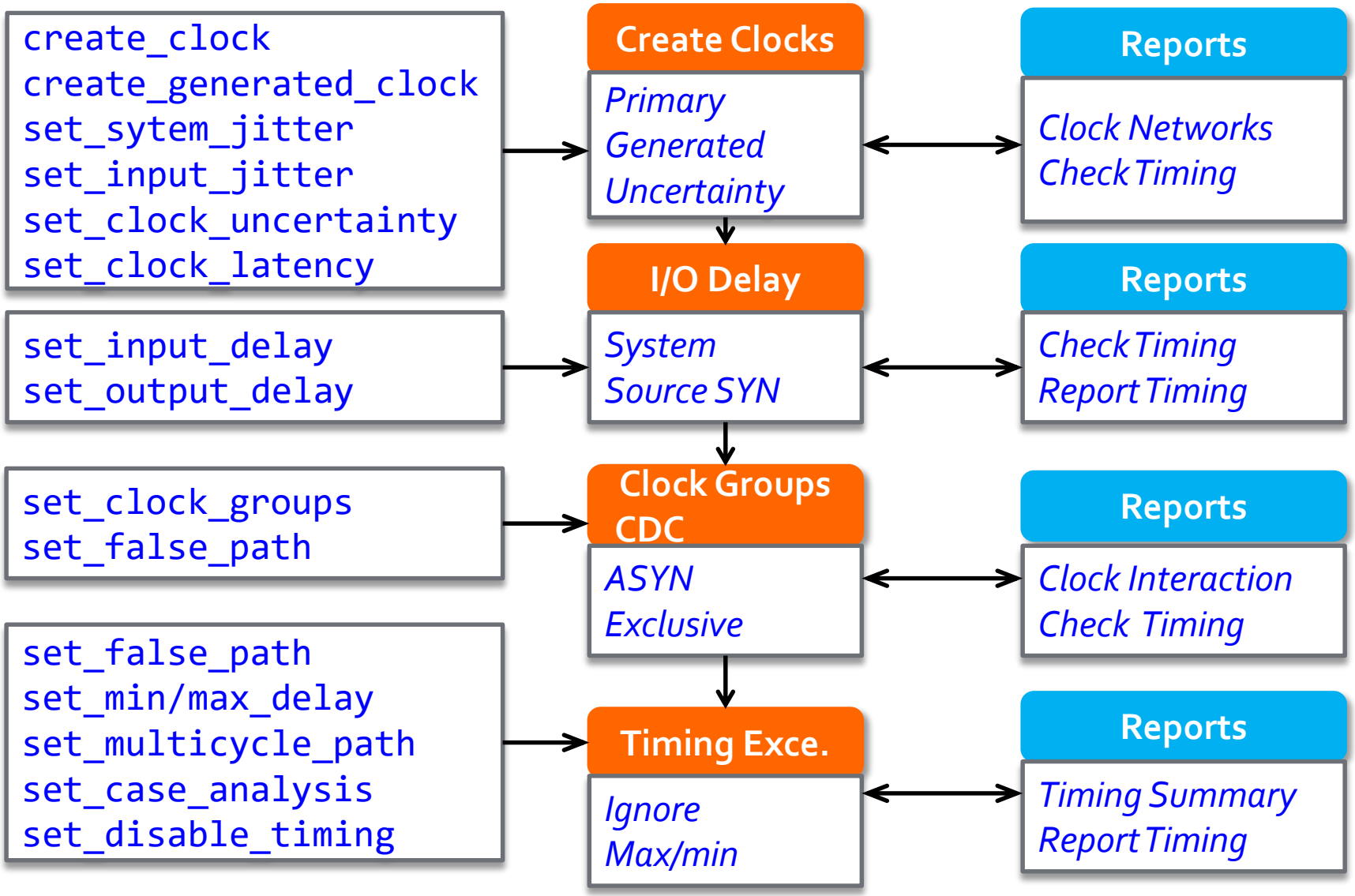
- **Some IP come with their own XDC constraints**
  - Example: The clocking wizard

The clocking wizard XDC will be read before the user XDC by default
(user constraints can override IP defined clocks by default)

- **The order of constraint files matters!**
  - To report the order of XDC files: `report_compile_order -constraints`
  - Always verify the clocks using `report_clocks`
  - To change the default processing order

    `set_property set_processing_order` ***`early|late`*** *`IP_XDC_File`*
  - If necessary, *IP_XDC_files* can be enabled/disabled

Defining Timing Constraints in Four Steps



Create Synthesis Constraints

- The net delay modeling is approximate and does not reflect placement constraints or complex effects such as congestion
- The main objective is to obtain a netlist which meets timing, or fails by a small amount, with realistic and simple constraints
- Synthesis constraints must use names from the elaborated netlist, preferably ports and sequential cells
  - During elaboration, some RTL signals can disappear and it is not possible to attach XDC constraints to them
- Once synthesis has completed, Xilinx recommends that you review the timing and utilization reports to validate that the netlist quality meets the application requirements and can be used for implementation

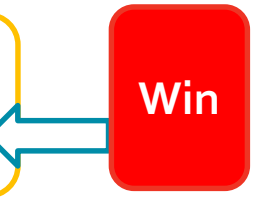
Create Synthesis Constraints

- **The synthesis engine accepts all XDC commands, but only some have a real effect**
  - Timing constraints related to setup/recovery analysis influence the QoR
    - create_clock, create_generated_clock
    - set_input_delay , set_output_delay
    - set_clock_groups, set_false_path, set_max_delay, set_multicycle_path
  - Timing constraints related to hold and removal analysis are ignored during synthesis
    - set_false_path -hold
    - set_min_delay
    - set_multicycle_path -hold

Recommended Constraints Sequence

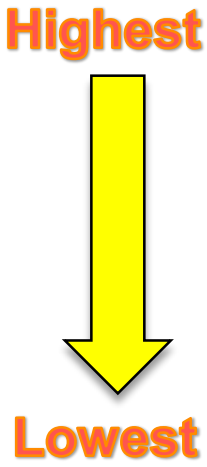
- XDC is based on Tcl syntax and interpretation rules. Like Tcl, XDC is a sequential language
- Variables must be defined before they can be used
  - Similarly, timing clocks must be defined before they can be used in other constraints
- For equivalent constraints that cover the same paths and have the same precedence, the last one applies

```
create_clock -name clk1 -period 10 [get_ports clk_in]
create_clock -name clk2 -period 11 [get_ports clk_in]
```

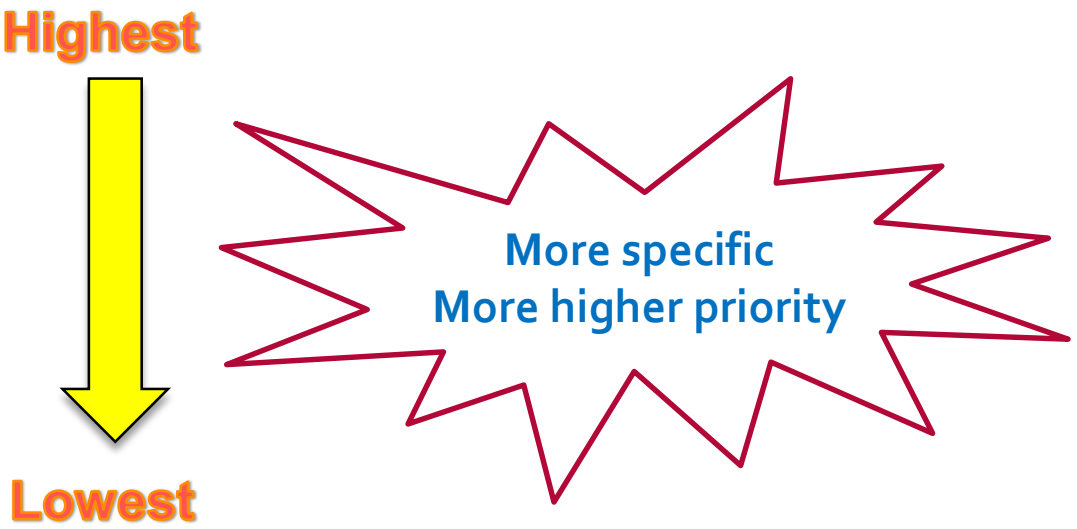


Timing Exceptions Priority

- Clock Groups (set_clock_groups)
- False Path (set_false_path)
- Max/min Delay Path (set_max/min_delay)
- Multicycle Paths (set_multicycle_path)



- The precedence rule for the filters, from highest to lowest
  - -from -through -to
  - -from -to
  - -from -through
  - -from
  - -through -to
  - -to
  - -through



Example

```
set_max_delay 12 -from [get_clocks clk1] -to [get_clocks clk2]
set_max_delay 15 -from [get_clocks clk1]
```

Win

```
set_max_delay 4 -through [get_pins inst0/I0]
set_max_delay 5 -through [get_pins inst0/I0] –through \
[get_pins inst1/I3]
```

Win

√

You must avoid using several timing exceptions on the same paths, so that the timing analysis results are not dependent on priority rules, and it is easier to validate the effect of your constraints