Vivado从此开始（To Learn Vivado From Here）

本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用

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- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

- 内容翔实全面：涵盖Vivado所有基本功能
- 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- 描述图文并茂：给出具体操作步骤，易于快速动手实践

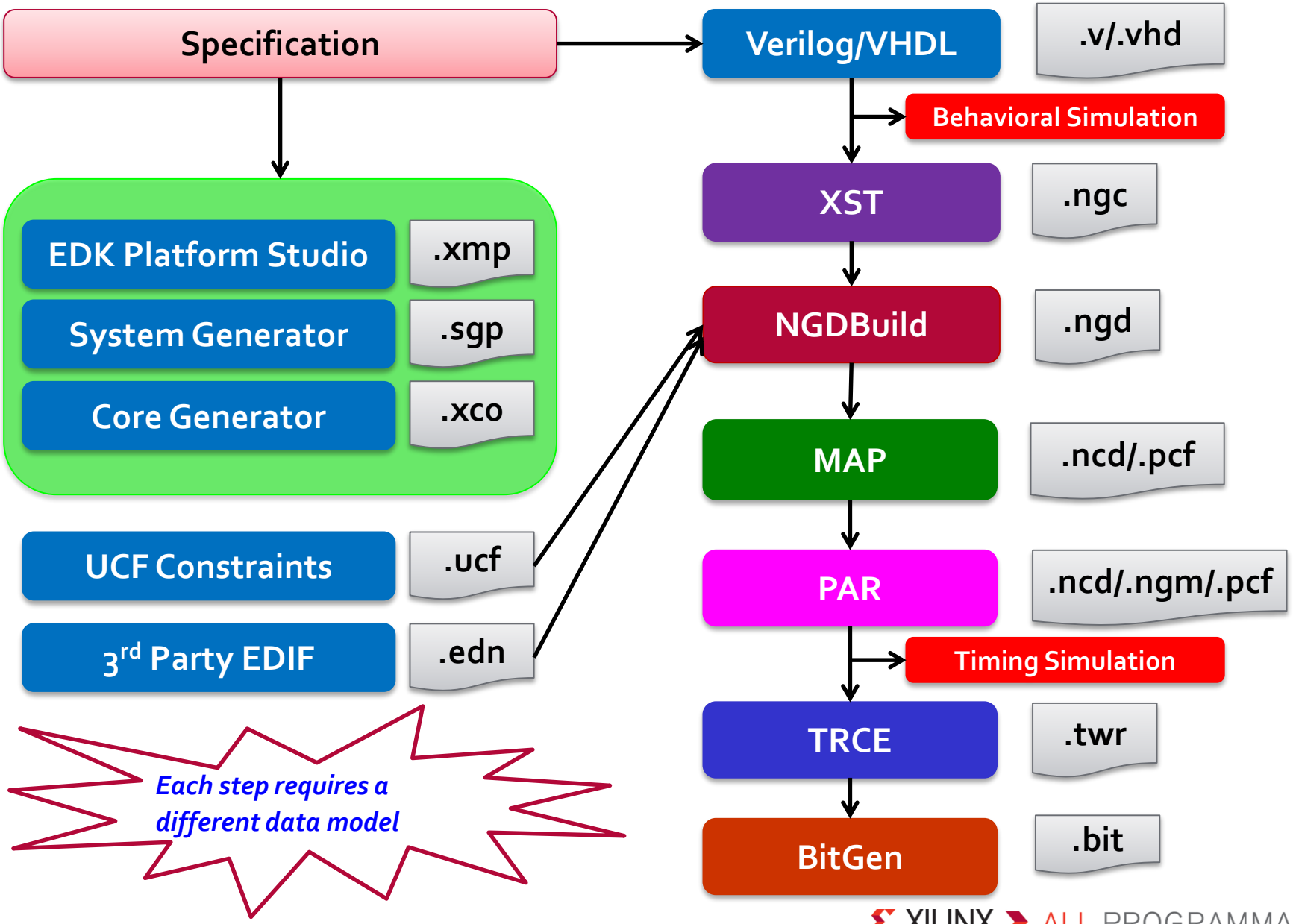
Vivado Design Flow Overview

Lauren Gao

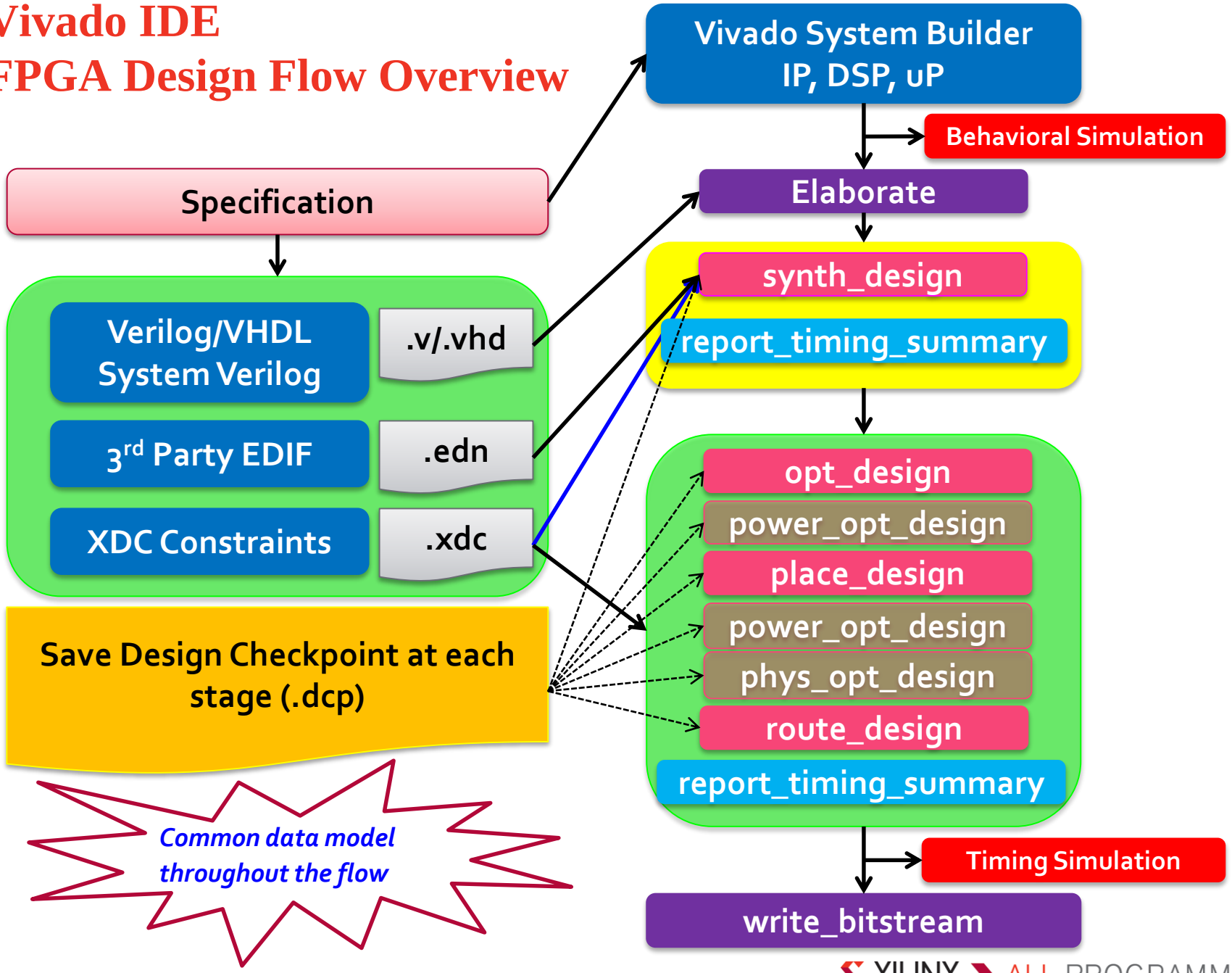
Agenda

- The difference of FPGA design flow between ISE and Vivado
- Vivado use modes
- Demonstrate project mode design flow features

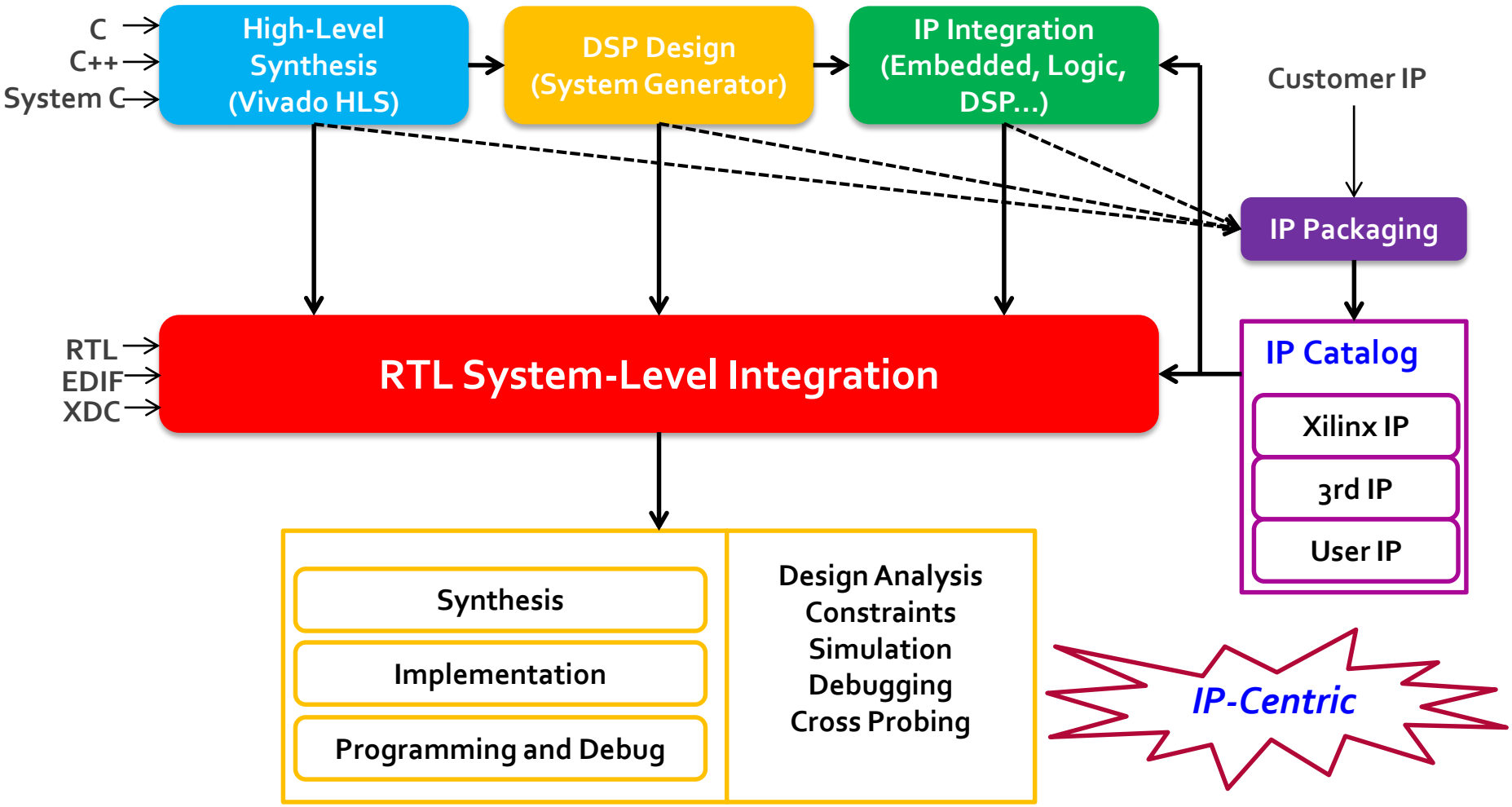
ISE Tools FPGA Design Flow Overview



Vivado IDE
FPGA Design Flow Overview



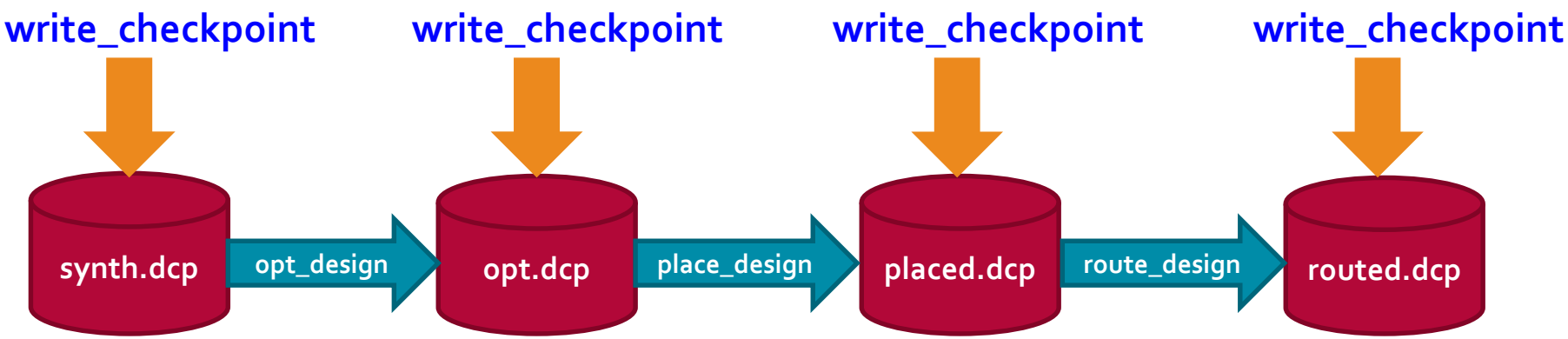
Vivado System Builder – System Level Design Flow



What is a Design Checkpoint?

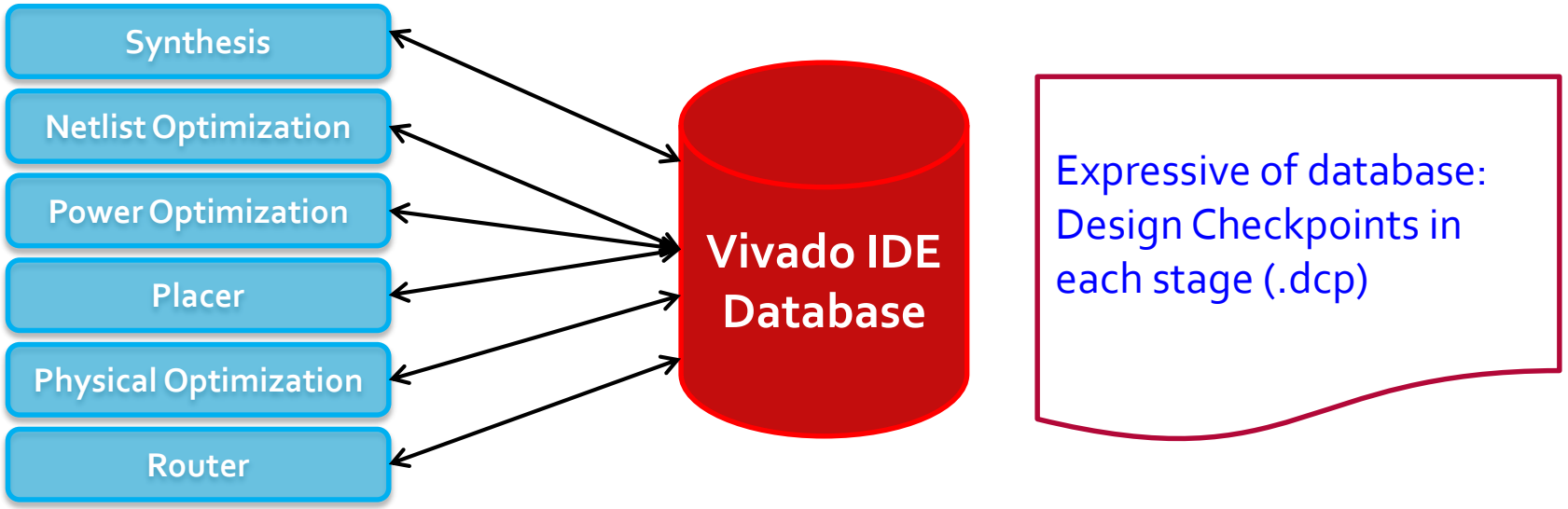
- **Everything needed to save and restore the current design**
  - Logical Netlist (EDIF)
  - Constraints (XDC)
  - Physical Data (XDEF)
- **Checkpoint uses**
  - Design progress
  - Design analysis
  - Design exploration

Design Checkpoint :
Synthesis: top.dcp
Opt: top_opt.dcp
Place: top_placed.dcp
Route: top_routed.dcp
Tcl commands:
write_checkpoint
read_checkpoint

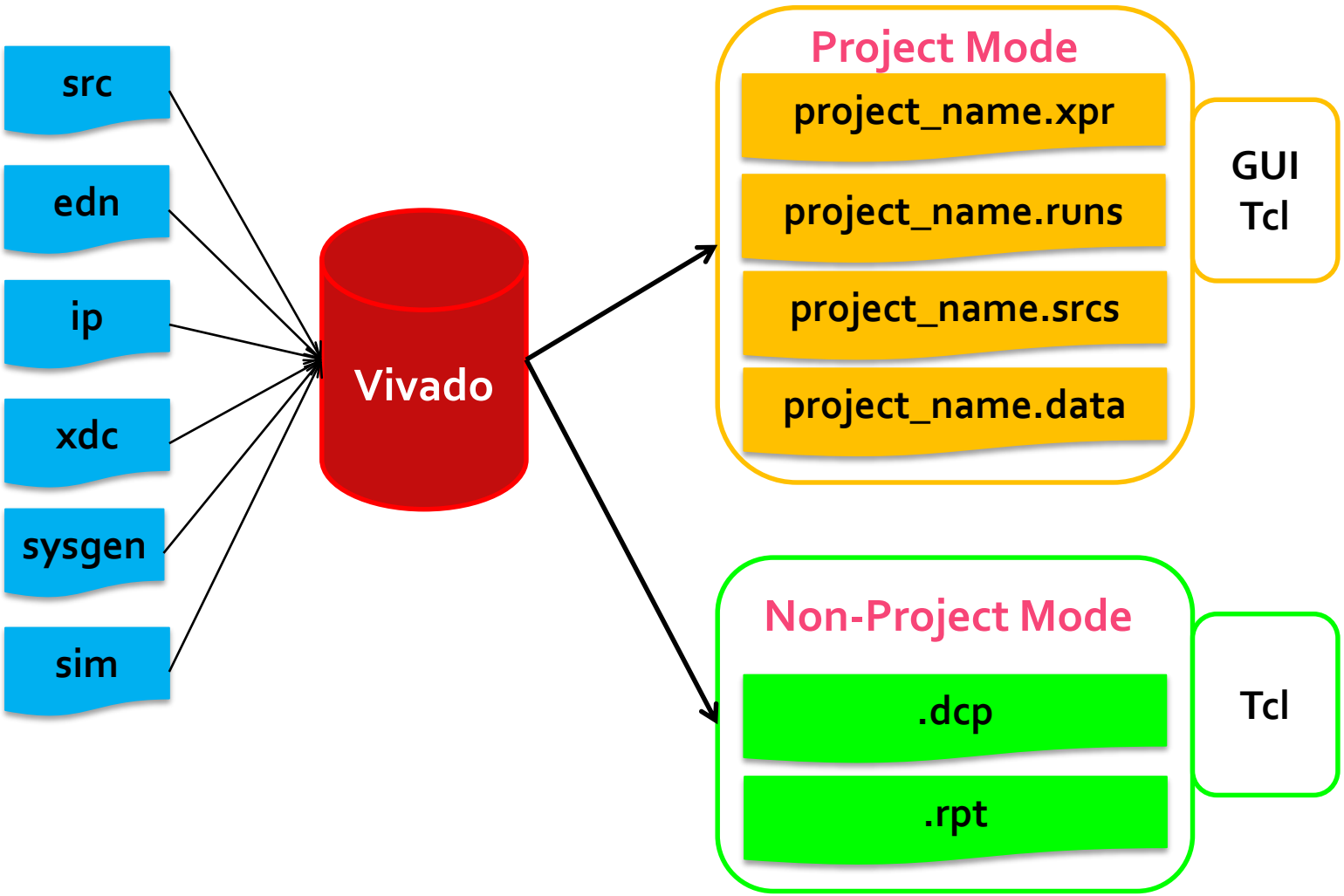


Design Database

- **Processes access the underlying database of your design**
  - Each process operates on a netlist and will modify the netlist or create a new netlist
- **Different netlists are used throughout the design process**
  - Elaborated
  - Synthesized
  - Implemented



Vivado Design Entry and Use Model



Project Data

- **All project data is stored in a project_name directory containing the following**
  - *project_name.xpr* file: Object that is selected to open a project (Vivado IDE project file)
  - *project_name.runs* directory: Contains all run data
  - *project_name.srcs* directory: Contains all imported local HDL source files, netlists, and XDC files
  - *project_name.data* directory: Stores floorplan and netlist data

Using the Project Mode Flow

- **Project mode advantages**
  - Source file management
  - Automatic design process and data management
  - Integrated IP design solution
  - Configure and manage multiple runs with varying strategies
  - Cross-probing to RTL
  - Consolidated messaging and tracking of design state
  - Interactive design analysis and constraints assignment
  - Full Tcl support

Using the Non-Project Mode Flow

- **Non-Project mode advantages**
  - Powerful and flexible Tcl based environment
  - Straight-forward compilation style flow
    - Common data model – all processing done in memory
    - Save design checkpoints at will
    - Powerful Tcl API – design and tool configuration, robust reporting
  - Use the integrated design environment GUI as needed
    - Design analysis, constraints assignment, implementation results
    - I/O plannning, floorplanning, debug core insertion
    - Perform implementation changes

Demo: Project Mode Design Flow

Summary

- **IP-Centric system level design integration**
  - Create and package IP and add it to IP catalog
  - Create IP subsystems with IP Integrator
    - Embedded processor, DSP, HLS
- **System design entry through hardware validation flows**
  - Advanced design, analysis and process management capabilities
- **Flexible use models**
  - Tcl accessible common data model throughout the flow
  - Project and compilation style flows
  - Support for third party software tools

More Info

- Ug888: design flows overview