Vivado从此开始（To Learn Vivado From Here）

本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用

作者：高亚军（Xilinx战略应用高级工程师）

- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

- 内容翔实全面：涵盖Vivado所有基本功能
- 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- 描述图文并茂：给出具体操作步骤，易于快速动手实践

Design Analysis After Synthesis Part I

Lauren Gao

Agenda

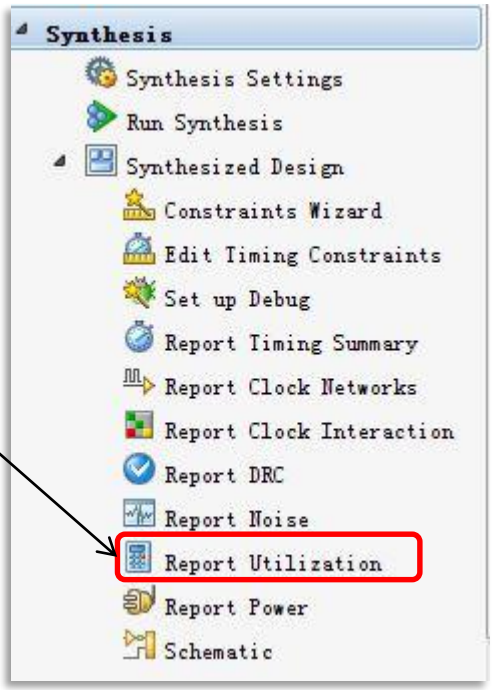
- Resource Utilization Analysis
- Clock Analysis
- Fanout Analysis
- Control Sets Analysis

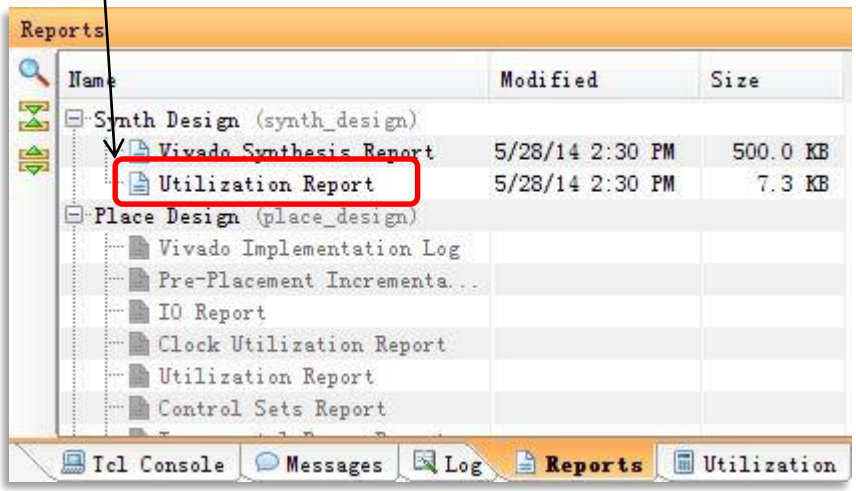
Resource Utilization Analysis

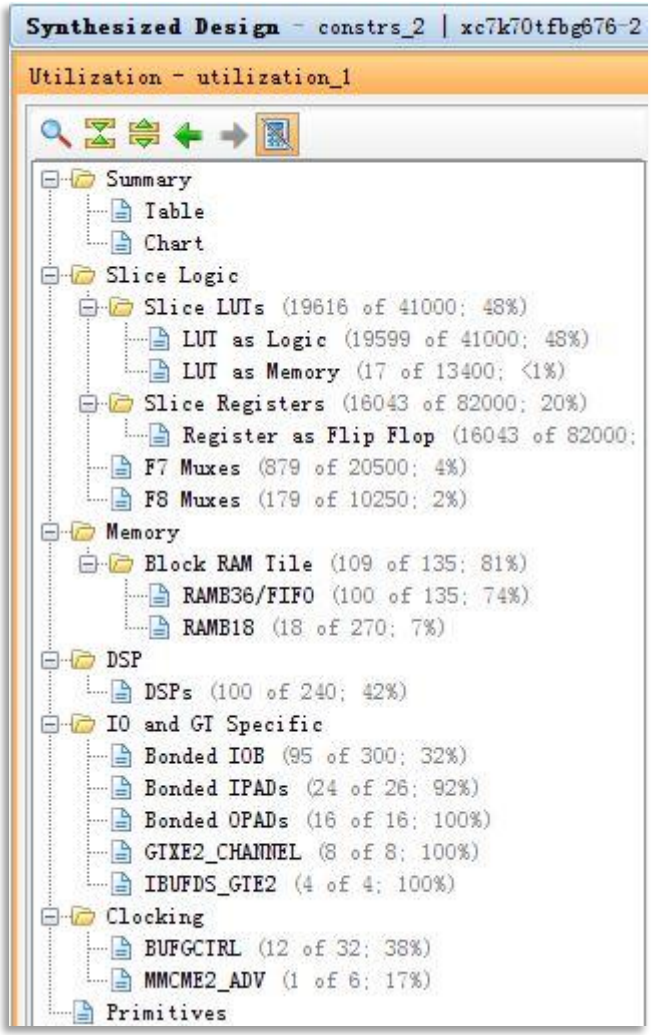
- Get resource utilization by GUI
- Get resource utilization by Tcl
- Get total resource utilization
- Get the resource utilization of the specified cells or pblocks

Resource Utilization by GUI

Open Synthesized Design







Report Utilization by Tcl

report_utilization [**-file** *arg*] [**-append**] [**-pblocks** *args*] [**-cells** *args*] [**-return_string**] [**-slr**] [**-packthru**] [**-name** *arg*] [**-no_primitives**] [**-omit_locs**] [**-hierarchical**] [**-hierarchical_depth** *arg*] [**-quiet**] [**-verbose**]

- **Top Resource Utilization**

```
report_utilization –name utilization_1
```

- **Save it in a File**

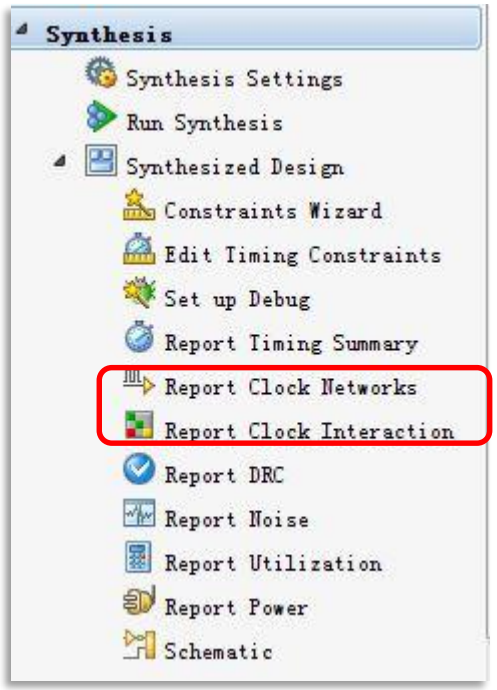
```
set mydir [get_property DIRECTORY [current_project]]
report_utilization -file $mydir/utilization.txt
```

- **Specified Cells**

```
set mycell [get_cells cpuEngine]
report_utilization -cells $mycell
report_utilization -pblocks [get_pblocks]
```

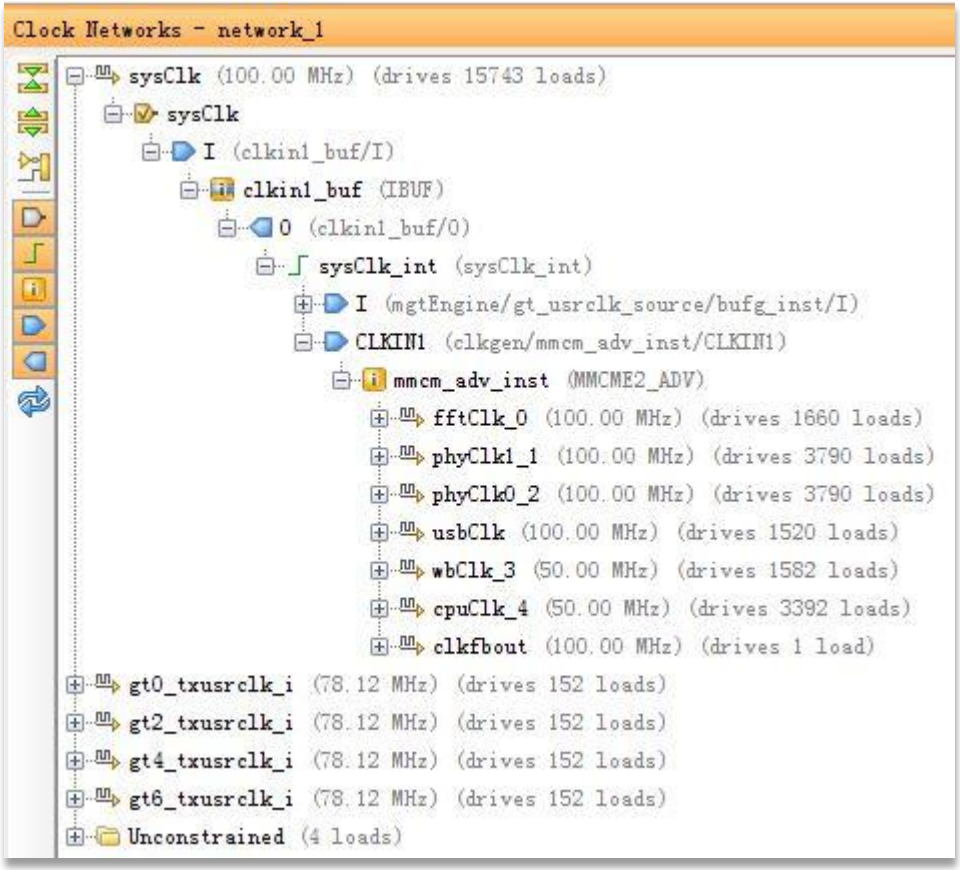
Clock Analysis

- Clock Networks
- Clock Interaction
- Clock Resource Utilization



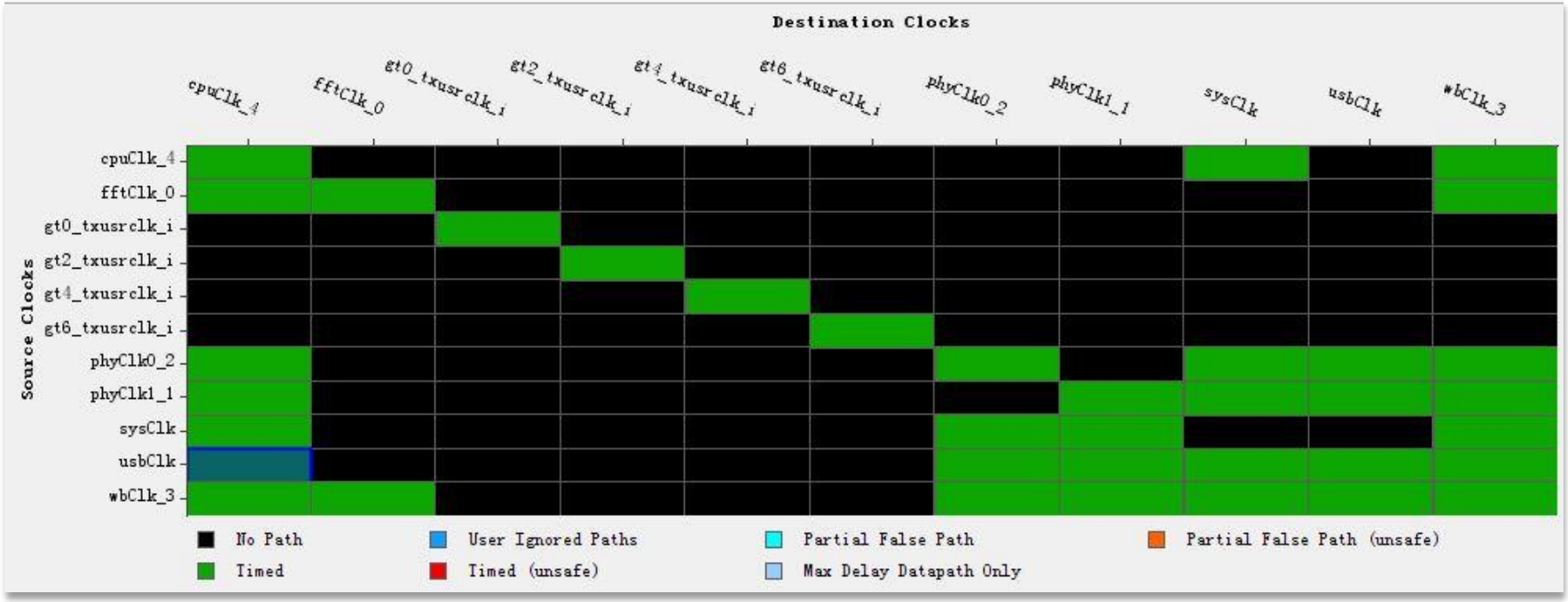
Clock Networks

- Reports the network fanout of each clock net in the design




```
report_clock_networks -name network_1
```

Clock Interaction



- Reports clock interactions and signals that cross clock domains to identify potential problems

```
report_clock_interaction -delay_type min_max \
-significant_digits 3 -name timing_2
```

Clock Utilization

- Returns information related to clock nets in the design and clock resource utilization on the target device

```
report_clock_utilization
```

Type	Used	Available	Num Locked
BUFG	12	32	0
BUFH	0	96	0
BUFIO	0	24	0
MMCM	1	6	0
PLL	0	6	0
BUFR	0	24	0
BUFMR	0	12	0

High Fanout Nets Analysis

report_high_fanout_nets [**-file** *arg*] [**-append**] [**-ascending**] [**-timing**] [**-histogram**] [**-load_types**] [**-clock_regions**] [**-slr**] [**-max_nets** *arg*] [**-min_fanout** *arg*] [**-max_fanout** *arg*] [**-name** *arg*] [**-cells** *args*] [**-return_string**] [**-quiet**] [**-verbose**]

```
report_high_fanout_nets -timing
```

Net Name	Fanout	Driver Type	Worst Slack(ns)	Worst Delay(ns)
reset_reg	10645	FDRE	8.665	0.466
usbEngine0/usb_dma_wb_in/buffer_fifo/fifo_out[0]	658	RAMB36E1	5.955	0.466
usbEngine1/usb_dma_wb_in/buffer_fifo/fifo_out[0]	658	RAMB36E1	5.955	0.466
usbEngine0/usb_dma_wb_in/buffer_fifo/fifo_out[1]	653	RAMB36E1	5.955	0.466
usbEngine1/usb_dma_wb_in/buffer_fifo/fifo_out[1]	653	RAMB36E1	5.955	0.466
usbEngine0/usb_dma_wb_in/buffer_fifo/fifo_out[2]	332	RAMB36E1	5.787	0.466
usbEngine1/usb_dma_wb_in/buffer_fifo/fifo_out[2]	332	RAMB36E1	5.787	0.466
cpuEngine/cpu_iwb_adr_o/buffer_fifo/O23	233	LUT6	-1.165	0.742
n_0_reset_reg_reg_rep	227	FDRE	7.885	0.416
cpuEngine/or1200_cpu/or1200_ctrl/O30[1]	221	FDCE	12.441	0.434

Control Sets Analysis

- Control sets are the list of control signals (Clock, CE, SR) for SLICE registers and LUTs
- Registers must belong to the same control set in order to be packed into the same device resource
- A high number of control sets can cause difficulty fitting the device and can cause routing congestion and timing issues

Report Control Sets

report_control_sets [**-file** *arg*] [**-append**] [**-sort_by** *args*]
[**-cells** *args*] [**-return_string**] [**-quiet**] [**-verbose**]

```
report_control_sets
```

Clock Enable	Synchronous Set/Reset	Asynchronous Set/Reset	Total Registers	Total Slices
No	No	No	2923	0
No	No	Yes	1727	0
No	Yes	No	818	0
Yes	No	No	566	0
Yes	No	Yes	4379	0
Yes	Yes	No	5630	0

Demo