

Vivado从此开始 (To Learn Vivado From Here)



本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用



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- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

- ◆ 内容翔实全面：涵盖Vivado所有基本功能
- ◆ 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- ◆ 描述图文并茂：给出具体操作步骤，易于快速动手实践



XILINX

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Design Analysis After Synthesis Part II

Lauren Gao

Working with Timing

➤ **get_timing_path:**

- Gets timing path objects that meet the specified criteria
- Create custom reporting and analysis
- *returns timing path objects which can be queried for properties, or passed to other Tcl commands for processing*

➤ **report_timing:**

- performs timing analysis on the specified timing paths of the current Synthesized or Implemented Design
- *returns a file or a string*

➤ **report_timing_summary, report_exception, reset_timing**

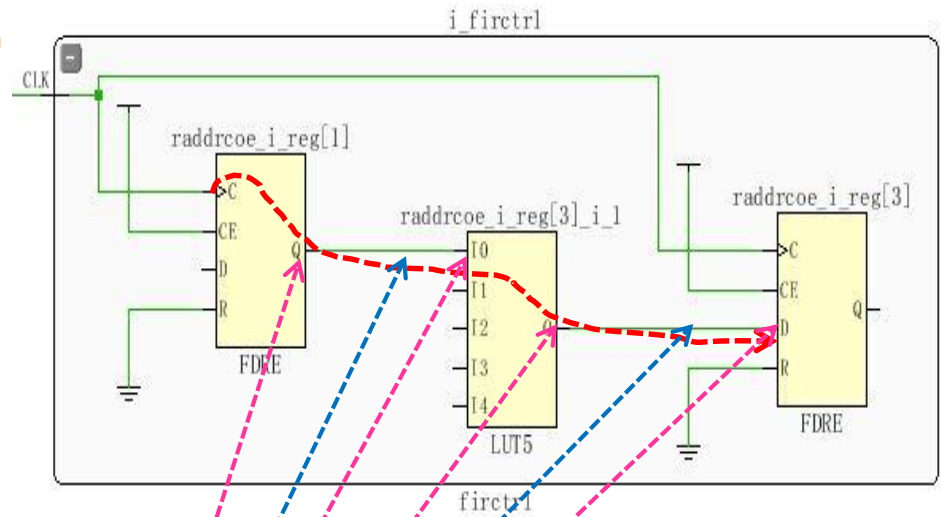
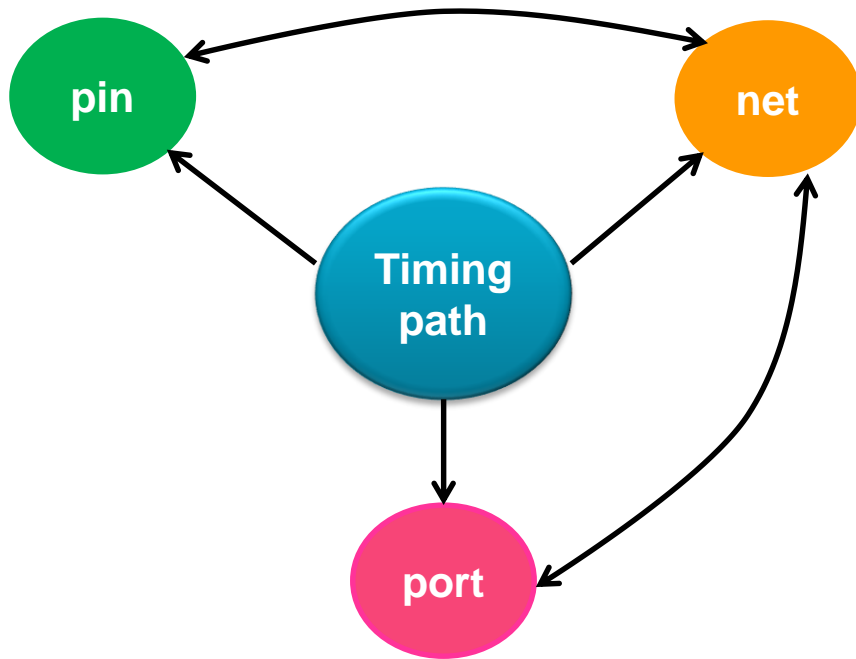
```
set paths [get_timing_paths -group clk_tx_clk_core_1 -max_paths 100]
report_timing -of_objects $paths
#Which is the equivalent of:
report_timing -group clk_tx_clk_core_1 -max_paths 100
```

get_timing_path

- **get_timing_paths** [-from *args*] [-rise_from *args*] [-fall_from *args*][-to *args*] [-rise_to *args*] [-fall_to *args*] [-through *args*][-rise_through *args*] [-fall_through *args*] [-delay_type *arg*][-setup] [-hold] [-max_paths *arg*] [-nworst *arg*] [-unique_pins][-slack_lesser_than *arg*] [-slack_greater_than *arg*] [-group *args*][-no_report_unconstrained] [-user_ignored] [-sort_by *arg*] [-filter *arg*][-regexp] [-nocase] [-match_style *arg*] [-quiet] [-verbose]
- -from/-to: ports, cells, pins, clock object
 - -through: pins, cells, nets
 - -delay_type: max == -setup
 - -delay_type: min == -hold
 - -slack_lesser_than: show path with expected slack
 - -max_path
 - -nworst
 - -unique_pins

report_timing has the similar options with this tcl command

Timing Path



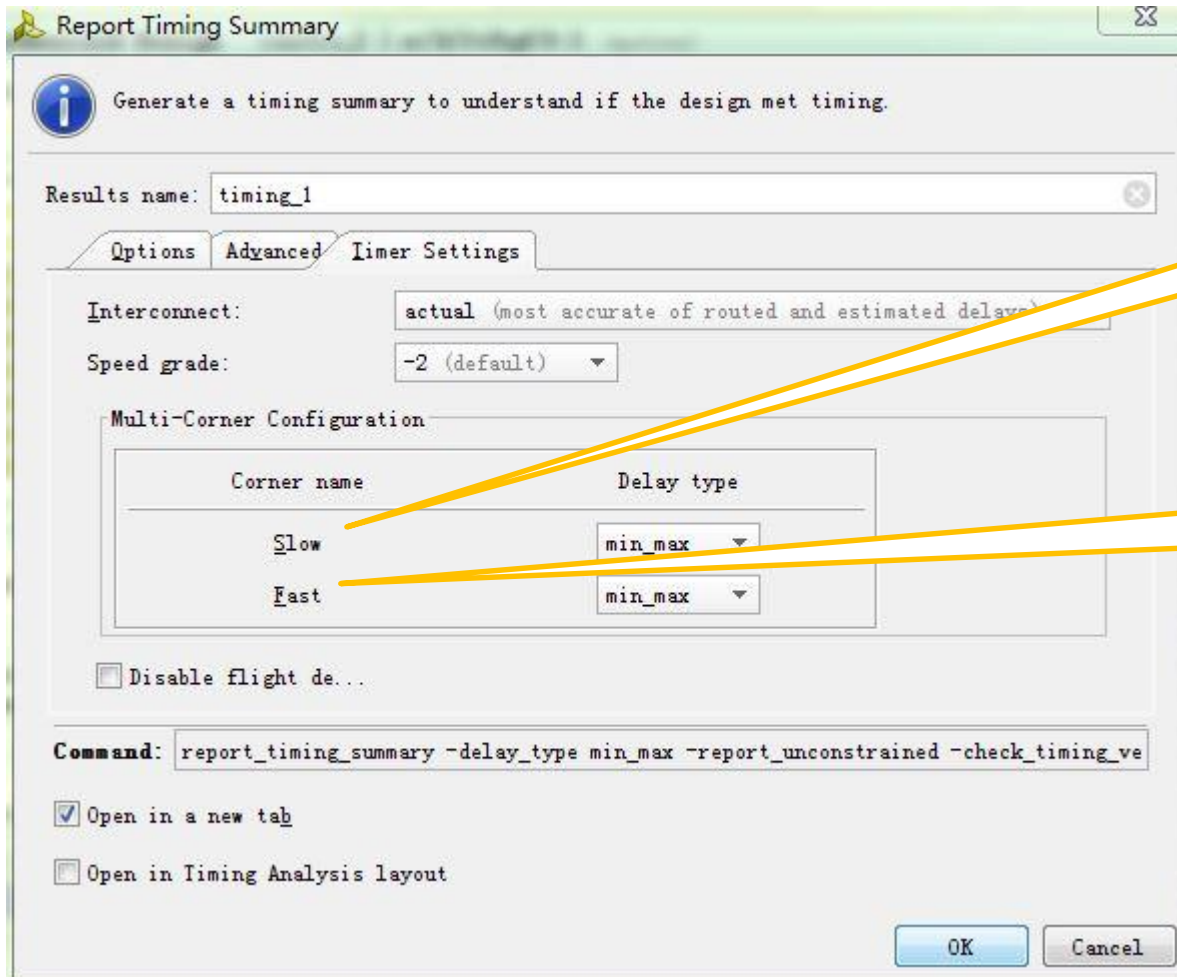
```
set mystart [get_cells {i_firctrl/raddrcoe_i_reg[1]}]
set myend [get_cells {i_firctrl/raddrcoe_i_reg[3]}]
set mypath [get_timing_path -from $mystart -to $myend -setup]
{i_firctrl/raddrcoe_i_reg[1]/C --> i_firctrl/raddrcoe_i_reg[3]/D}
set mynets [get_nets -of $mypath]
set mypins [get_pins -of $mypath]
```

Properties of Timing Path

```
report_property $mypath
Property      Type      Read-only  Value
CLASS         string   true       timing_path
CLOCK_PESSIMISM  double  true       -0.668
CORNER        string   true       Slow
DATAPATH_DELAY double   true       1.424
DELAY_TYPE    string   true       max
ENDPOINT_CLOCK clock   true       clk_out1_clk_gen
ENDPOINT_CLOCK_DELAY double  true       -2.640
ENDPOINT_PIN   pin      true       i_firctrl/raddrcoe_i_reg[3]/D
EXCEPTION     string   true
GROUP         string  true       clk_out1_clk_gen
LOGIC_LEVELS  int    true       1
NAME          string   true       {i_firctrl/raddrcoe_i_reg[1]/C --> i_firctrl/raddrcoe_i_reg[3]/D}
REQUIREMENT  double  true       20.000
SKEW         double  true       -0.029
SLACK       double  true       18.348
STARIPPOINT_CLOCK clock  true       clk_out1_clk_gen
STARIPPOINT_CLOCK_DELAY double  true       -3.279
STARIPPOINT_PIN pin      true       i_firctrl/raddrcoe_i_reg[1]/C
UNCERTAINTY   double  true       0.084
```



Multi-Corner Configuration



Slow: low voltage,
high temp

Fast: low temp,
high voltage

setup checks will fail
at slow process
corner, and hold
checks at fast

Demo