Vivado从此开始（To Learn Vivado From Here）

本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用

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- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

- 内容翔实全面：涵盖Vivado所有基本功能
- 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- 描述图文并茂：给出具体操作步骤，易于快速动手实践

Manage IP Constraints

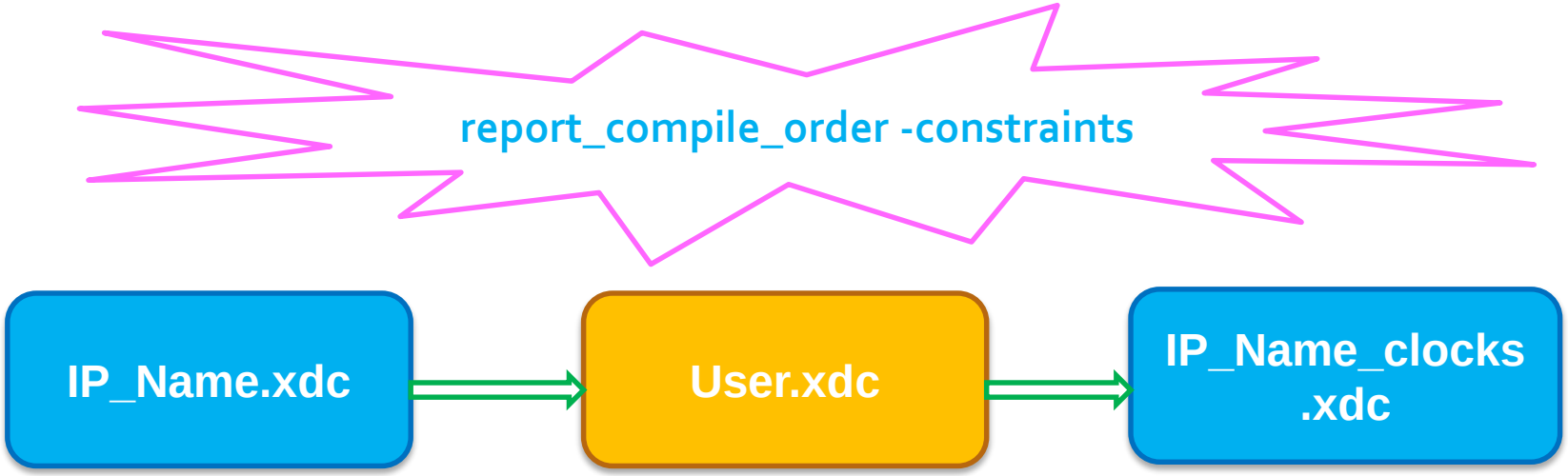
Lauren Gao

XDC Files Generated By IP

- An IP can deliver a number of XDC files
  - **<IP_Name>.xdc**
    - Clock creation commands as well as all commands without outside clock dependencies
  - **<IP_Name>_clocks.xdc**
    - All commands with dependencies to outside clocks
  - **<IP_Name>_ooc.xdc**
    - Default top level clock definitions. Used during creation of Synthesized Design Checkpoint (DCP)
  - <IP_Name>_board.xdc
    - Board Specific physical constraints
  - Possibly additional XDC files for synthesis or implementation only

Constraint File Processing Order

- By default, the Vivado IDE processes the core XDC files <IP_Name.xdc> before any user constraints
- By default, the Vivado IDE processes the <IP_Name>_clocks.xdc file after user constraints and other IP core XDC files
- <IP_Name>_ooc.xdc is only used in the DCP creation when using the recommended default flow (IP synthesized OOC to the top-level design)



Constraints Created for IP During Flow

- **dout_touch.xdc**
  - Used during the creation of the Synthesis Design Checkpoint (.DCP)
  - Contains commands to set dont_touch properties on the IP top
  - Prevents the interface ports from being removed

Will see this being read in the Log for the IP design Run

Constraints Created for IP During Flow

- **<IP Name>_in_context.xdc**
  - This file is created and stored in the IP DCP file, in the following conditions:
    - The IP output any clocks
    - The IP has an instance of I/O buffers
  - It is processed before the end-user constraints
  - It is not necessary during implementation because the IP are no longer a black box

Will see this being read in the global synthesis log file

Demo