Vivado从此开始（To Learn Vivado From Here）

本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用

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- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

- 内容翔实全面：涵盖Vivado所有基本功能
- 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- 描述图文并茂：给出具体操作步骤，易于快速动手实践

Using Design Rule Checks in Vivado

Lauren Gao

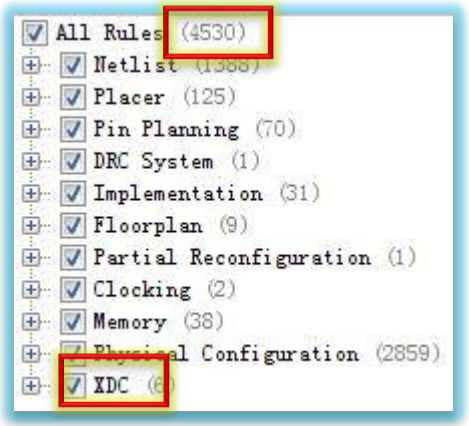
DRC Methodology

- Always run DRC early in the flow
- Run DRC after each major design step
  - After Elaborate
  - After Synthesis
  - After Implementation
- Fix Critical Warnings and Errors before proceeding to next step

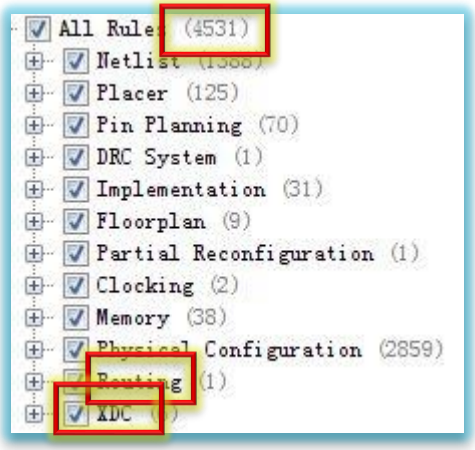
Rule Decks

Elaborated Design

Synthesized Design

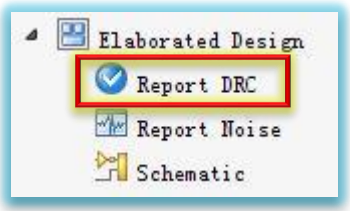


Implemented Design

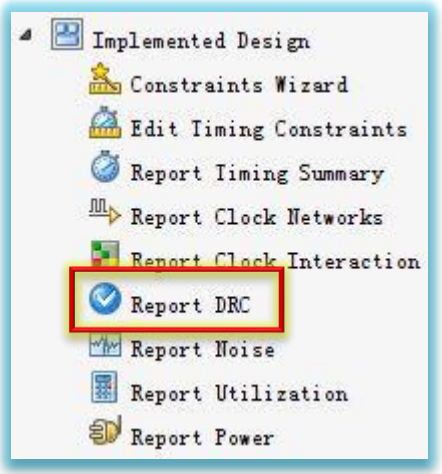


Invoking Methodology Check

Design Stages	methodology_checks		timing_checks
	RTL	XDC	
Elaborated Design	√	√	
Synthesized Design		√	√
Implemented Design		√	√



Tcl:
`report_drc`



DEMO

Summary

- Always run DRC early in the flow
- Run DRC after each major design step
- Fix Critical Warnings and Errors before proceeding to next step