Vivado从此开始（To Learn Vivado From Here）

本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用

作者：高亚军（Xilinx战略应用高级工程师）

- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

- 内容翔实全面：涵盖Vivado所有基本功能
- 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- 描述图文并茂：给出具体操作步骤，易于快速动手实践

Designing with IP

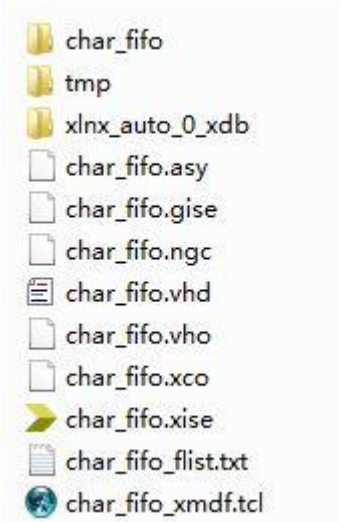
Lauren Gao

Agenda

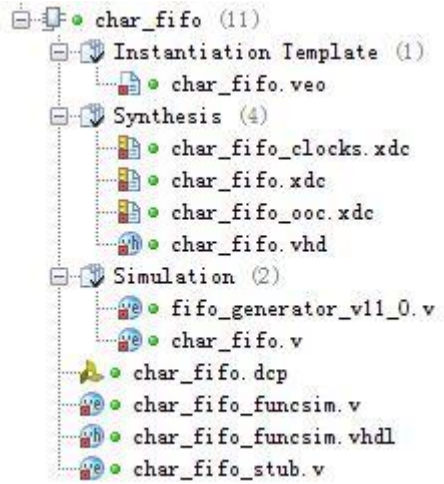
- **Vivado IP Overview**
- **Vivado IP Design Flow**
- **New Tool: IP Packager**
- **Demo:**
  - Project Based IP Design Flow
  - Manage IP Design Flow
  - Create and Package IP

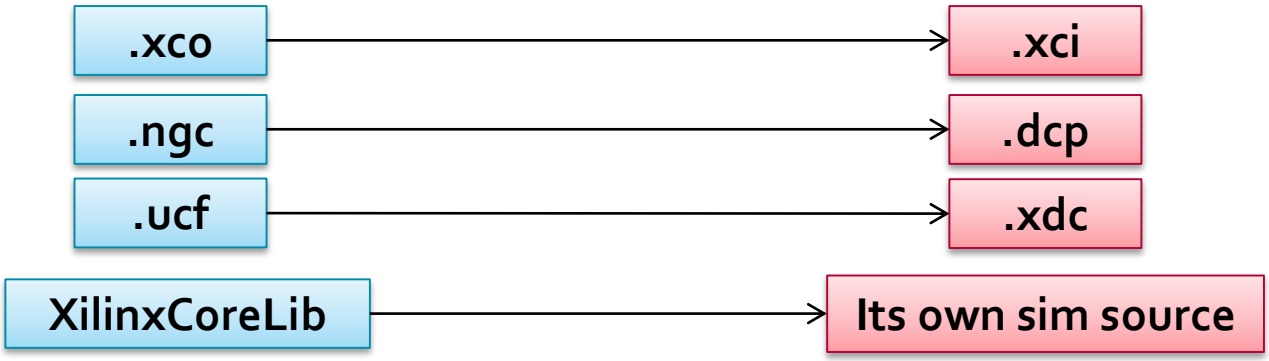
Vivado Design Suite IP vs ISE CORE Generator IP

IP in ISE



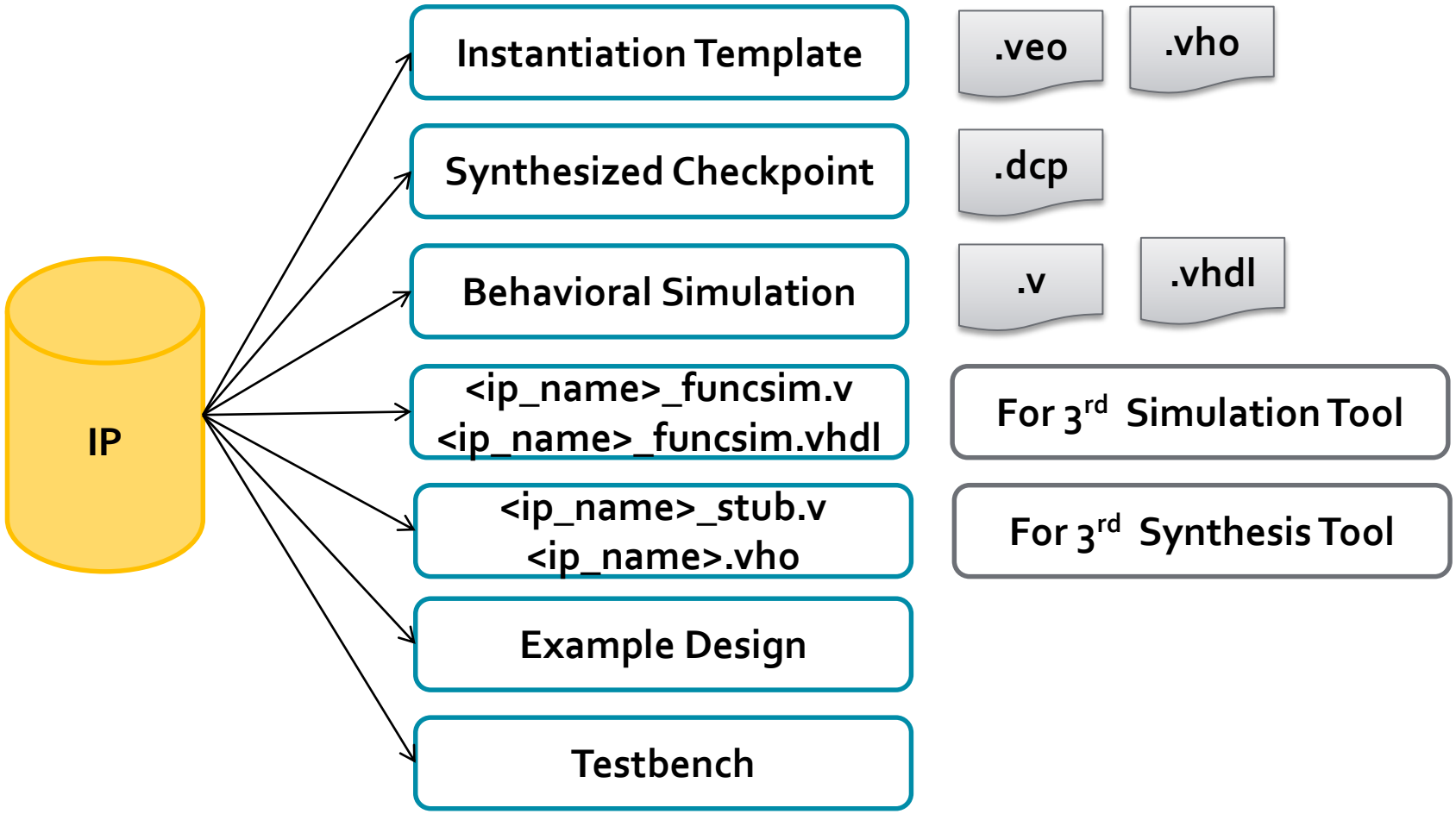
IP in Vivado





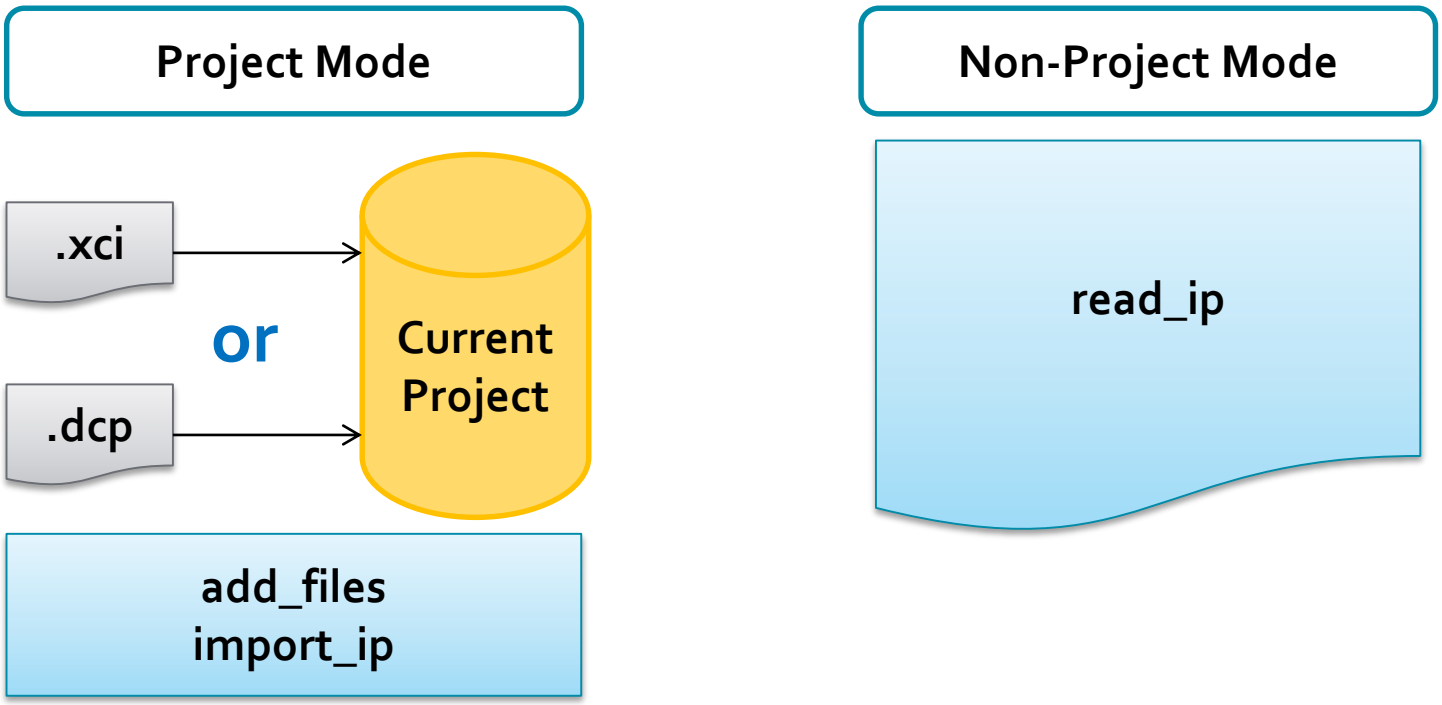
.dcp is not only the netlist but also constraints

IP Output Products in Vivado

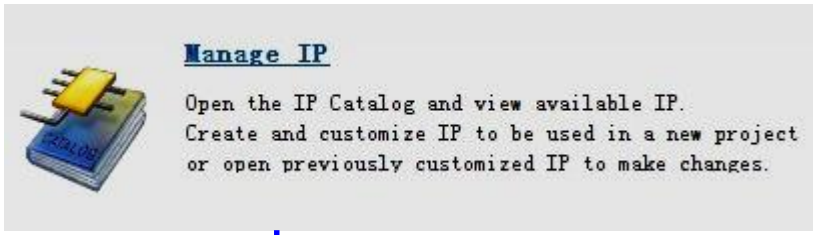


Flexible IP Use Models I Vivado

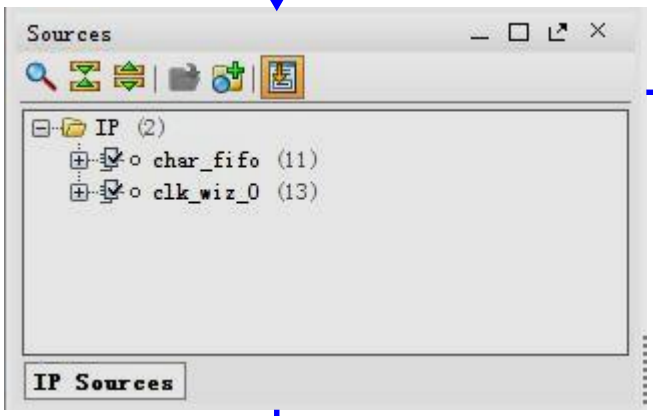
- Create standalone reusable IP locations
- Project based IP management
- Synthesize OOC or globally
- Lock IP to a specific version or update to current version

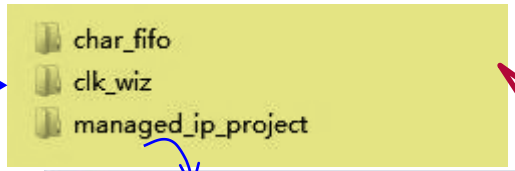


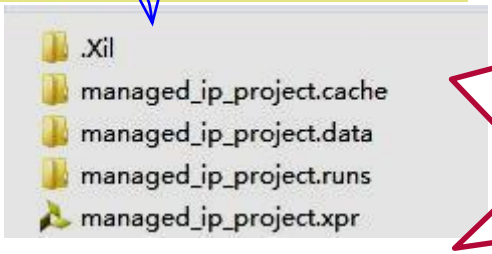
Create Standalone Reusable IP Locations



- **Add or Create Design Sources**
  Add .dcp to the project
- **Add Existing IP**
  Add .xci to the project

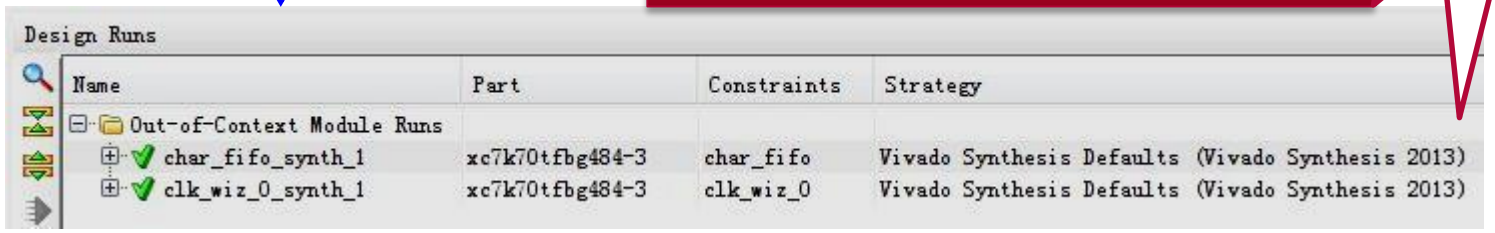






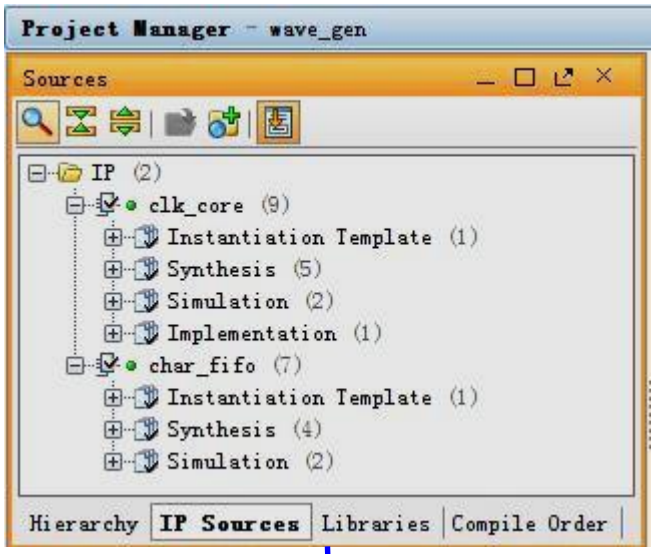
How to add IP to the project efficiently?

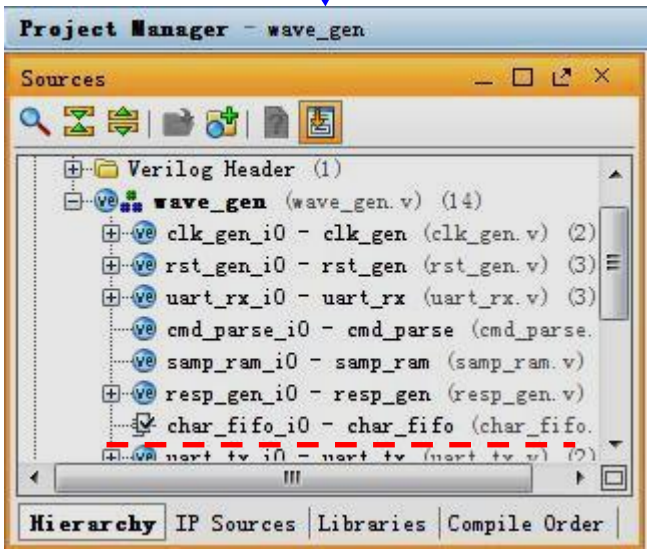
Each IP has its own directory

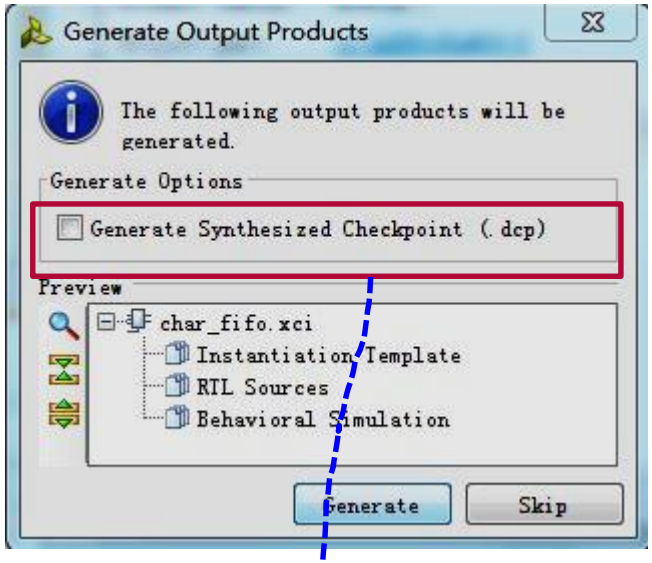


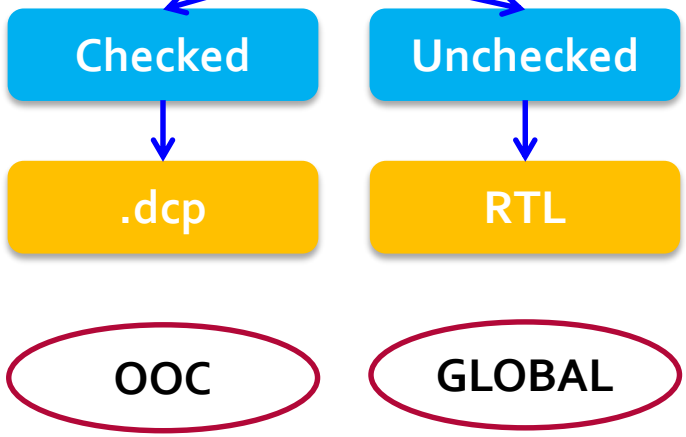
Tcl

Project Based IP Management

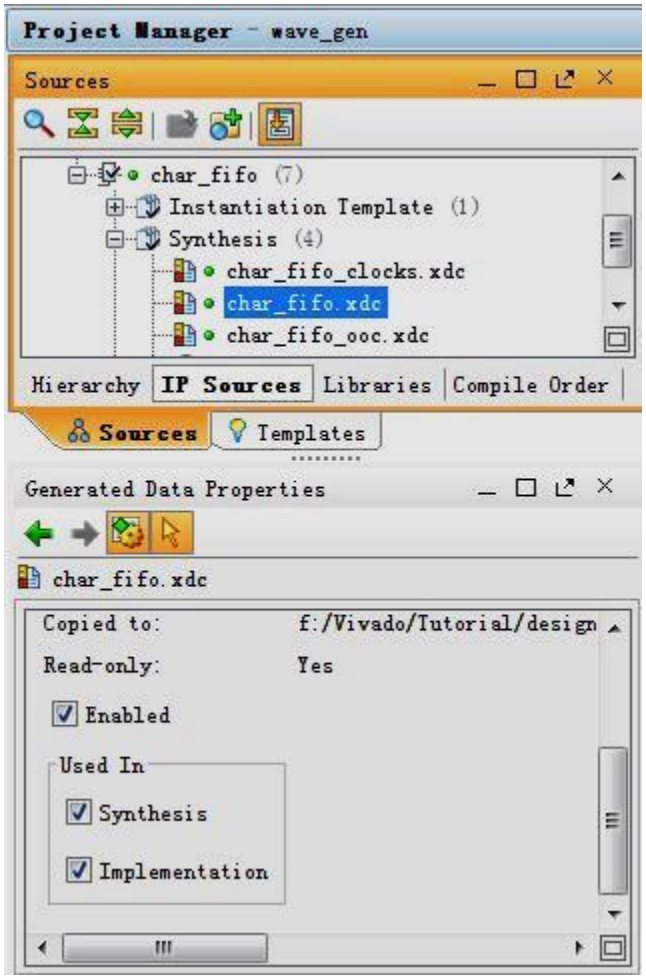








How to Deal with Generated XDC

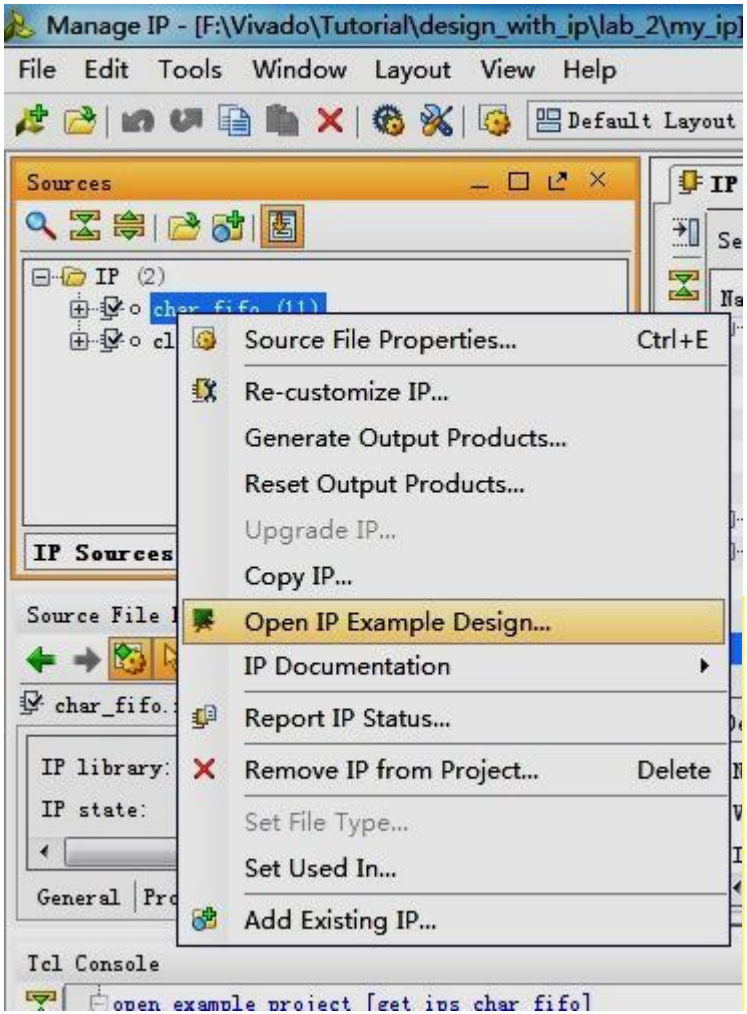


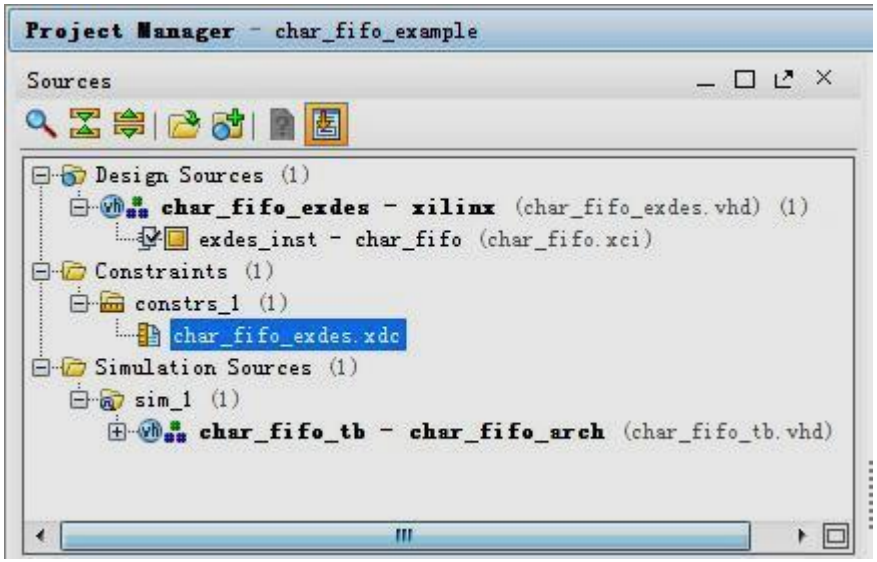
- In default, generated xdc is used in both Synthesis and Implementation.
- We donot need to do anything for it.
- report_compile_order -constraints

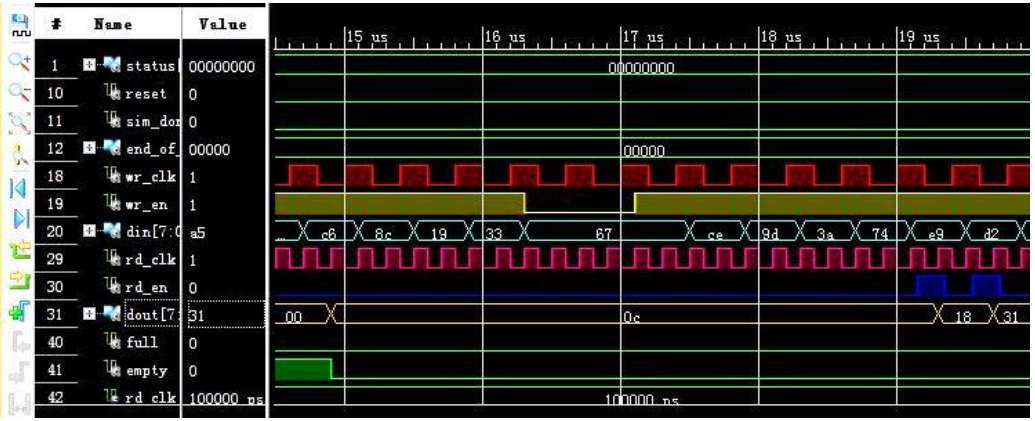
```
report_compile_order -constraints
INFO: [Vivado 12-3442] The output from report_compile_order is primarily targeted for human
Constraint evaluation order for 'synthesis' with filesets 'sources_1' & 'constrs_1':
```

Index	File Name	Used_In	Scoped_To_Ref	Scoped_To_Cells	Processing_Order
1	clk_core_board.xdc	Synth & Impl	clk_core	inst	EARLY
2	clk_core.xdc	Synth & Impl	clk_core	inst	EARLY
3	char_fifo.xdc	Synth & Impl	char_fifo	UO	EARLY
4	wave_gen_pins.xdc	Synth & Impl			NORMAL
5	wave_gen_timing.xdc	Synth & Impl			NORMAL
6	clk_core.dcp	Synth & Impl			NORMAL
7	char_fifo.dcp	Synth & Impl			NORMAL
8	char_fifo_clocks.xdc	Synth & Impl	char_fifo	UO	LATE

Open IP Example Design

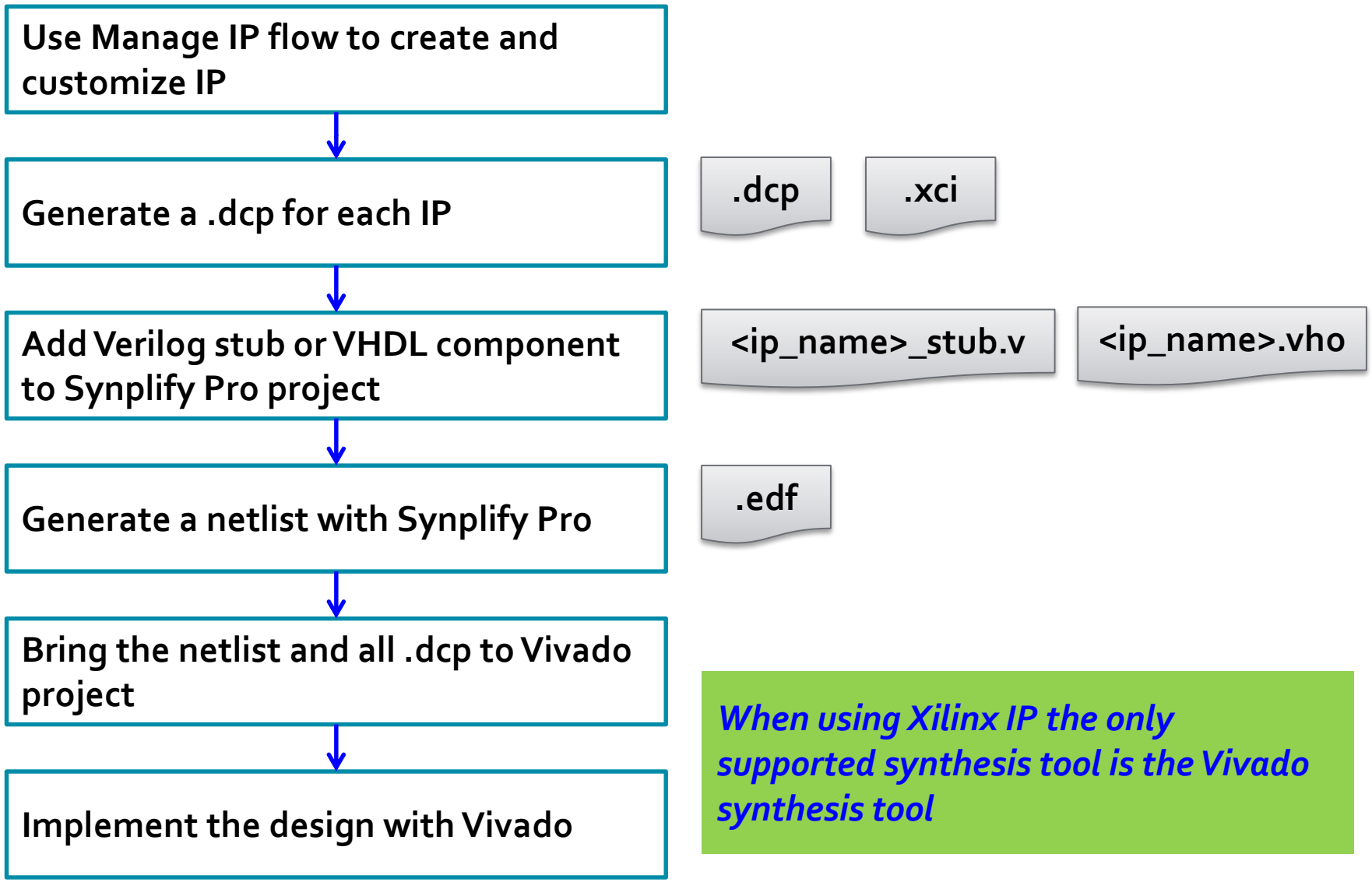






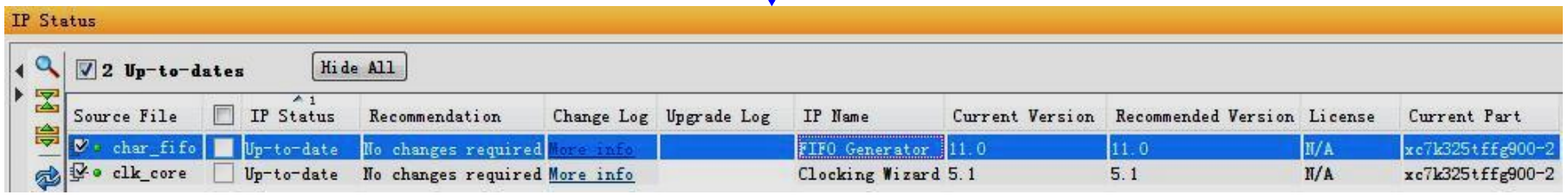
open_example_project [get_ips char_fifo]

Using Xilinx IP with 3rd Party Synthesis Tools



IP Version Control

report_ip_status -name ip_status_1



report_property [get_ips char_fifo]

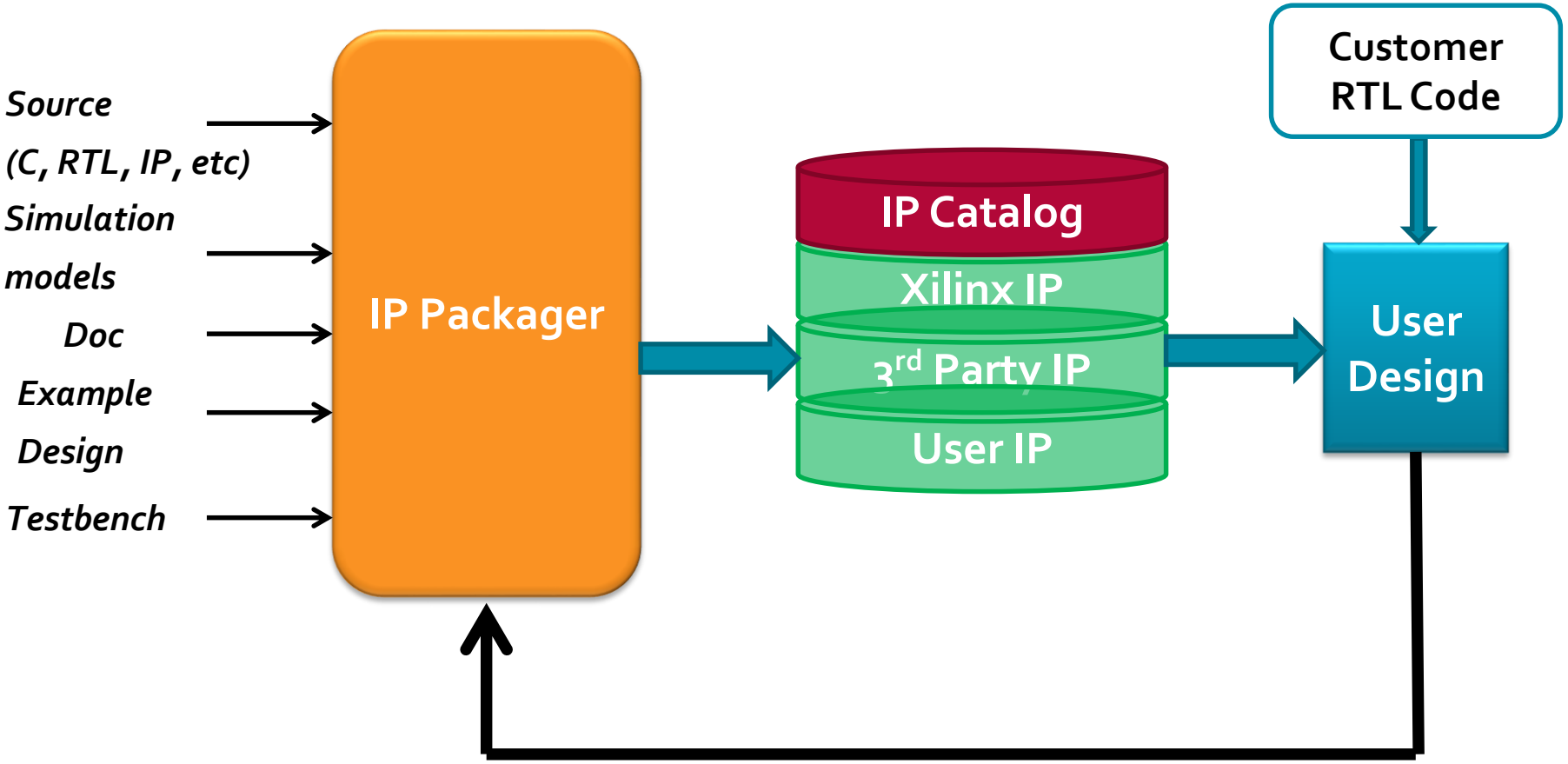
DELIVERED_TARGETS	string*	true	instantiation_template synthesis simulation
DESIGN_TOOL_CONTEXTS	string*	true	HDL IPI Sysgen
IPDEF	string	true	xilinx.com:ip:fifo_generator:11.0
IP_DIR	string	true	f:/Vivado/Tutorial/design_with_ip/lab_2/my_ip/char_fifo
IP_FILE	string	true	f:/Vivado/Tutorial/design_with_ip/lab_2/my_ip/char_fifo/char_fifo.xci
IP_OUTPUT_DIR	string	false	f:/Vivado/Tutorial/design_with_ip/lab_2/my_ip/char_fifo
IS_LOCKED	bool	false	0
IS_MANAGED	bool	false	1
IS_NATIVE	bool	true	1
KNOWN_TARGETS	string*	true	simulation synthesis example instantiation_template
NAME	string	true	char_fifo
STALE_TARGETS	string*	true	
SUPPORTED_TARGETS	string*	true	instantiation_template synthesis simulation example
SW_VERSION	string	true	2013.3
SYNTHESIS_FLOW	string	true	OUT_OF_CONTEXT

Some Tcl Commands about IP

- **Get a list of IPs in the current design**
  - get_ips
- **Generate target data for the specified source**
  - generate_target
- **Open the example project for the indicated IP**
  - open_example_project
- **Reset target data for the specified source**
  - reset_target
- **Upgrade a configurable IP to a later version**
  - upgrade_ip

More info: ug835

IP-Centric Design Flow



Demo

- Project Based IP Design Flow
- Manage IP Design Flow
- Create and Package IP