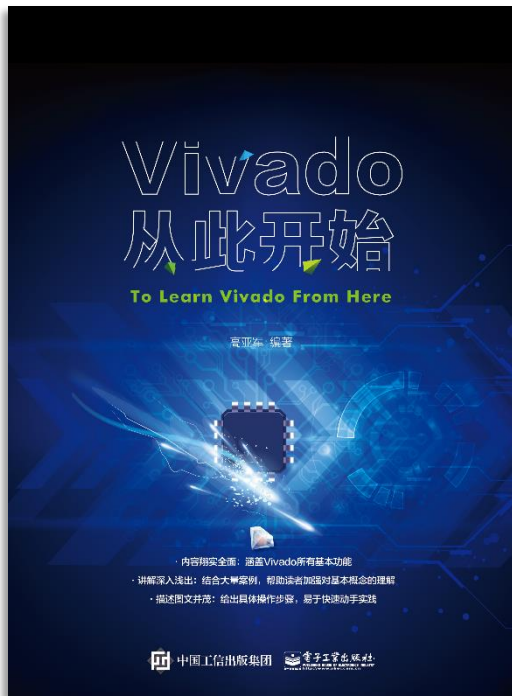


Vivado从此开始 (To Learn Vivado From Here)



本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用



作者：高亚军（Xilinx战略应用高级工程师）

- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

- ◆ 内容翔实全面：涵盖Vivado所有基本功能
- ◆ 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- ◆ 描述图文并茂：给出具体操作步骤，易于快速动手实践



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Timing Closure Part 1

Lauren Gao

Agenda

- Vivado Baseline Timing Constraint
- Timing Closure Tips

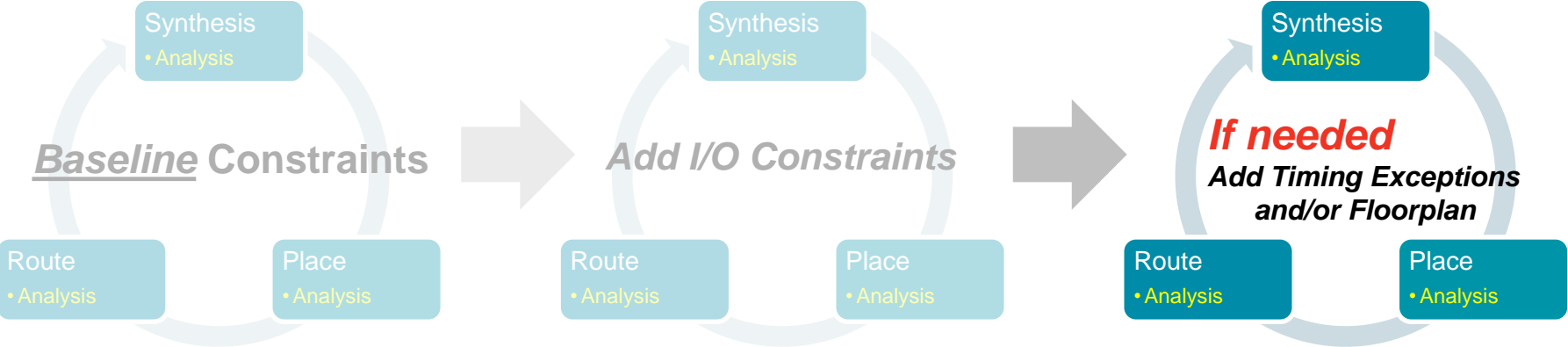
Addressing Vivado Timing Challenges

- **With ISE, many customers relied on SmartXplorer to close timing:**
 - Easy and effective in many cases
 - Downside -> lose timing closure skills
 - Cost Table has the nature of randomness
 - When to read timing report: **After Map**

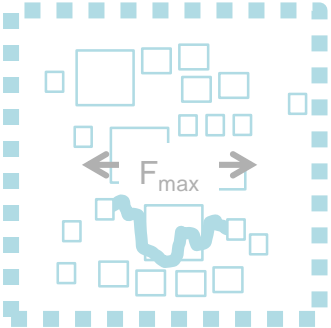
- **With Vivado “new” techniques have to be used**
 - Fundamental timing closure techniques have not changed
 - Customers just need a refresher: baselining the design
 - When to read timing report: **After Synthesis**

- **Vivado is extremely powerful for design analysis to determine the root cause of the timing issues**

Progressive Approach to Design Closure

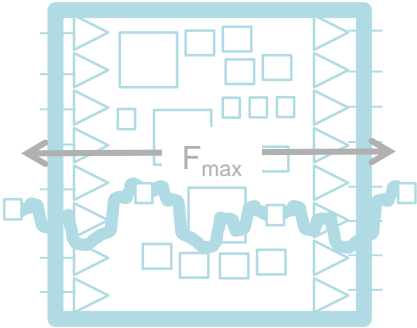


Optimize Internal Paths



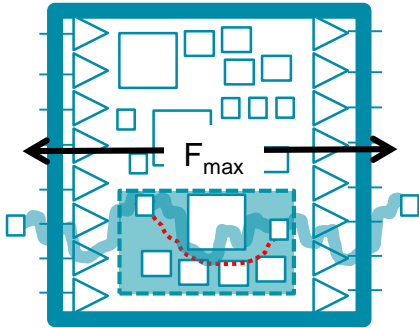
Baseline XDC

Optimize Entire Chip



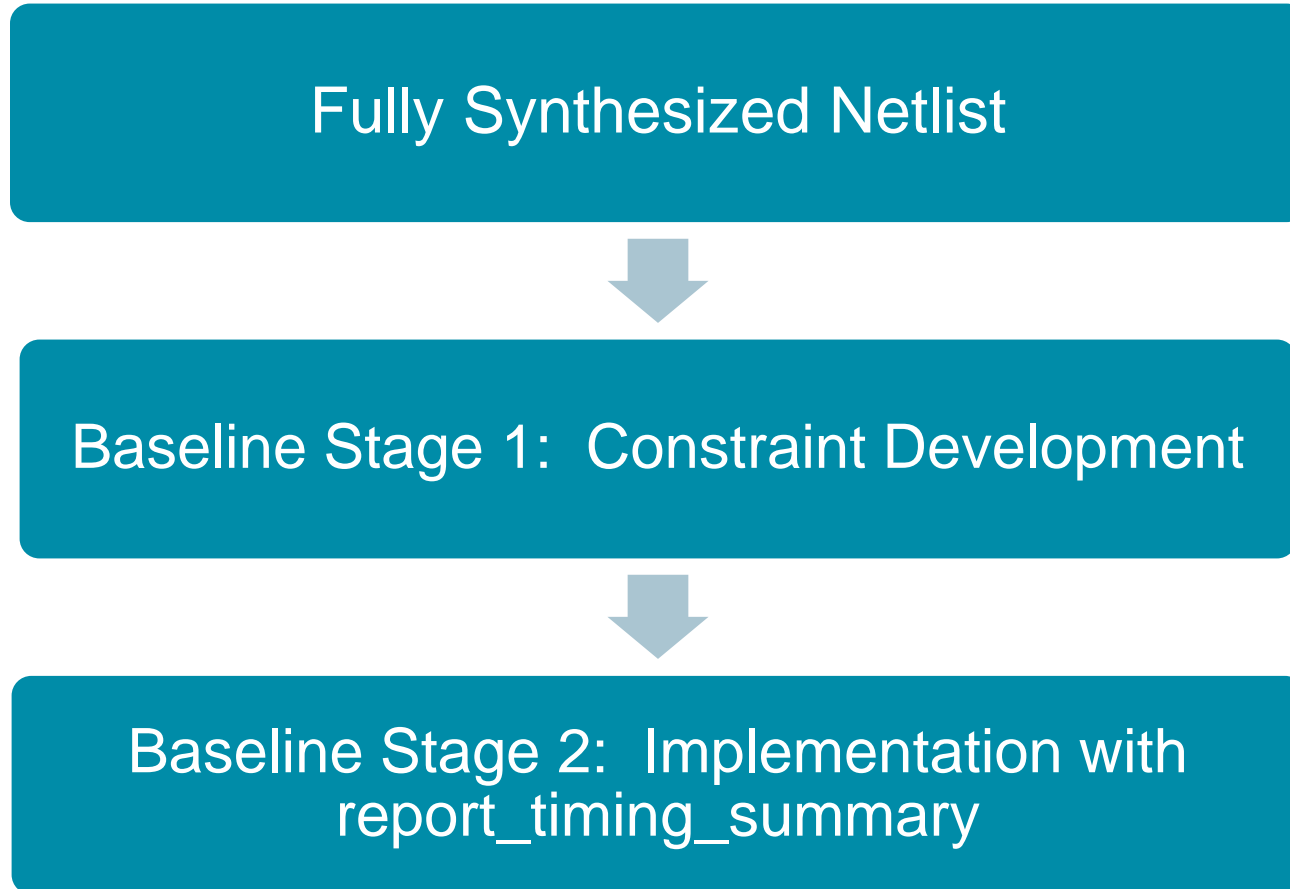
Complete XDC

Fine-tune



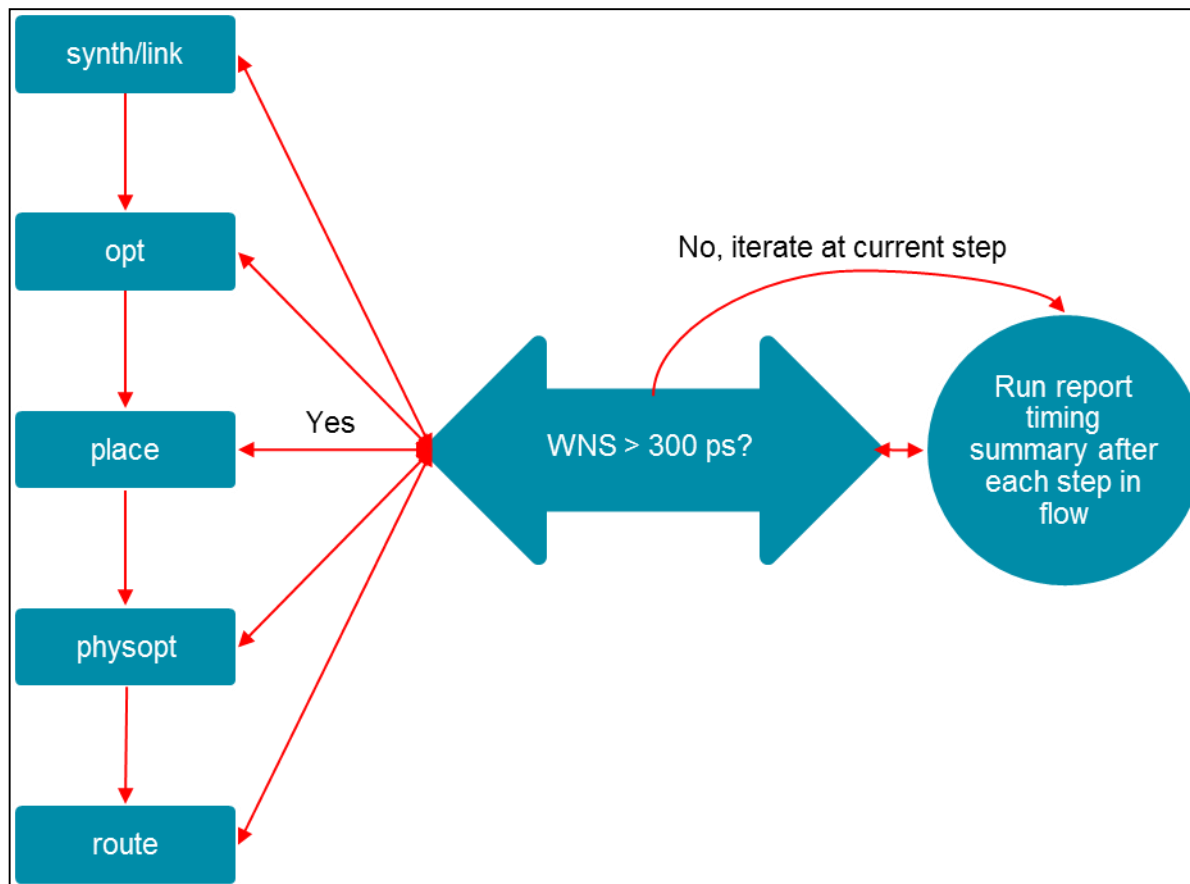
Final XDC

Baselining Customer Designs With Vivado



Baseline Stage 2

- Run **report_timing_summary** after each step (not optional)
- Ensure **WNS > 300 ps**



Developing Constraints From Scratch

➤ Q. How do I start?

➤ A. Open **synthesized design** in Vivado IDE

➤ Q. How do I make sure I'm starting from scratch?

➤ A. tcl_console> **reset_timing**

➤ Q. How do I know what to constrain?

➤ A. **report_clock_networks**

Developing Constraints From Scratch

- Q. How do I know when I'm done constraining clocks?
- A. When `report_clock_networks` shows no unconstrained networks

- Q. How do I make sure my clocks are correct?
- A. `report_clocks` shows period and waveform of every clock in the design

- Q. How do I know what clocks should be related?
- A. `report_clock_interaction -sort` by Common Primary Clock

DEMO