Vivado从此开始（To Learn Vivado From Here）

本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用

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- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

- 内容翔实全面：涵盖Vivado所有基本功能
- 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- 描述图文并茂：给出具体操作步骤，易于快速动手实践

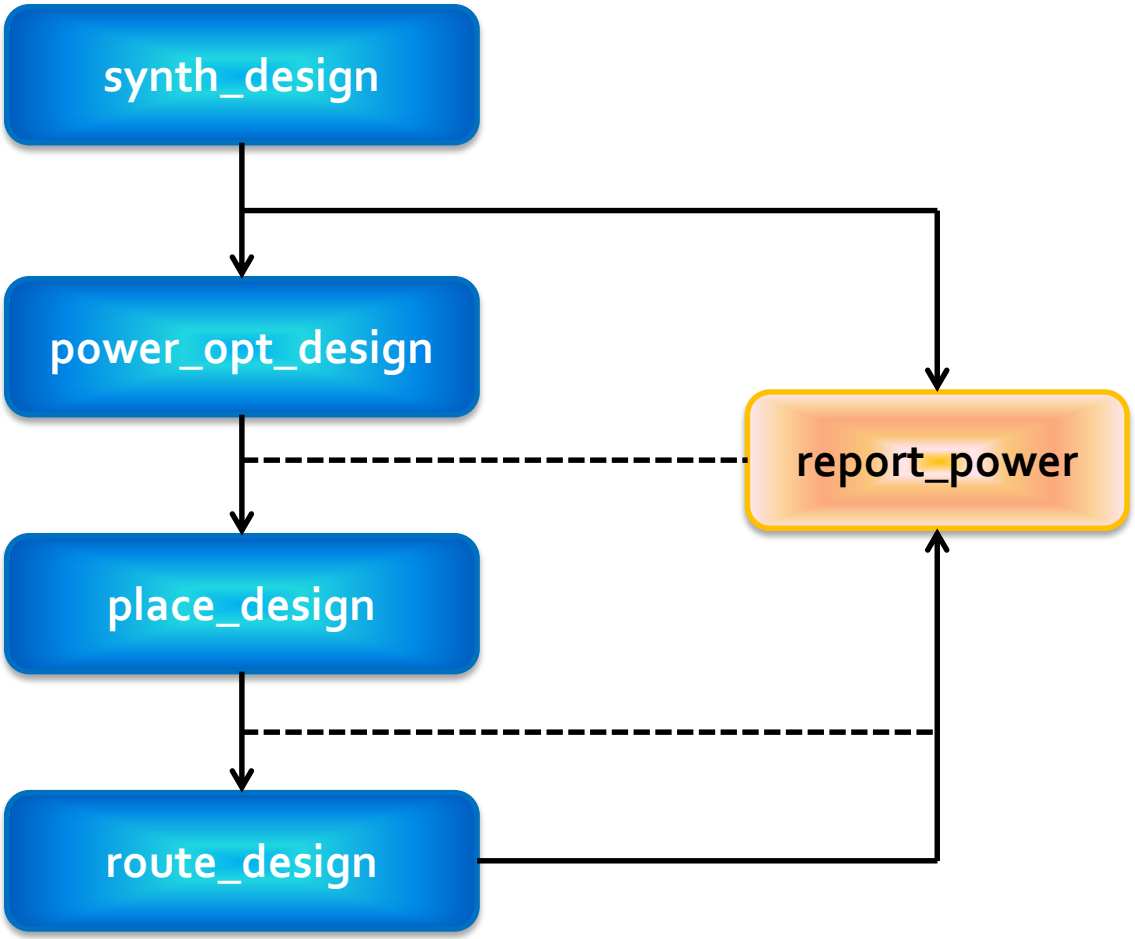
Power Estimation and Optimization

Lauren Gao

Power Estimation Flow in Vivado

- **Estimation power at various stages of design**
  - Post-synthesis to post-route
  - Higher accuracy reports after post-route
- **Two modes of power estimation**
  - Vector based (SAIF/VCD)
    - simulation activity file from real world operation
    - Recommended and fast estimation
  - Vectorless
    - Simpler input but relatively less accurate
    - Tool calculates probability of switch rate and %high

Report Power at Any Stage



Understanding Toggle Rates

- Toggle Rate reflects how often an output changes relative to a given clock
  - It can be modeled as a percentage between 0-200%
- Toggle rate: 100% , clock frequency: 100MHz, data frequency: 50MHz

Data Frequency = Toggle Rate * Clock Frequency/2

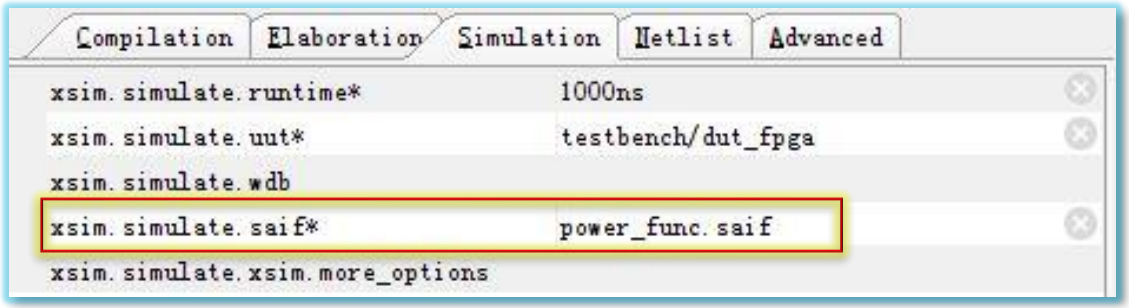
- Realistic toggle rates, along with loading a SAIF or VCD file should be used to achieve optimal power results

More info:

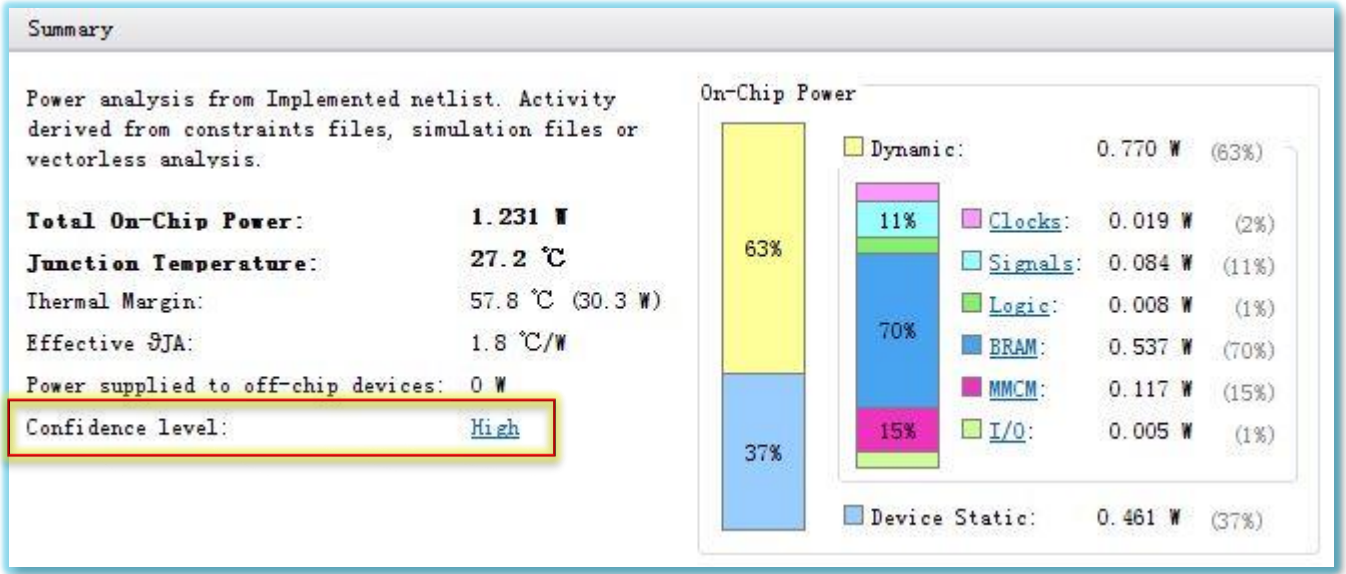
http://www.xilinx.com/itp/xilinx10/isehelp/xpa_c_togglerates.htm

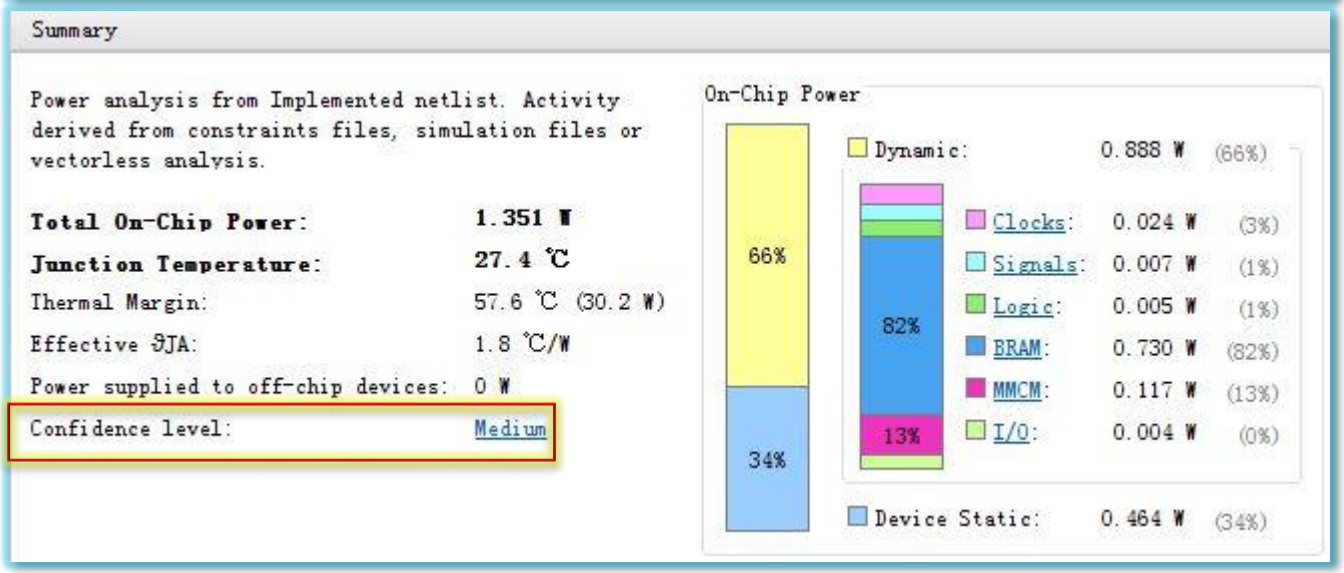
SAIF File

- Switching Activity Interchange Format
- It is an optional output file from simulation
- During simulation you can specify on which nodes to record switching activity
- The SAIF file was created to provide most of the information contained in a VCD file but in a much smaller size file
- Loading an SAIF file into Report Power will provide a more accurate power estimation



With/Without SAIF





Best Practices

- **Provide accurate device and environment information**
- **Supply SAIF input to tool if available**
  - Real activity of the chip and not corner case tests
  - At a minimum, capture RTL IO activity
- **Ensure all clocks are properly constrained in the design**
  - Unconstrained clock will be assumed to have a o MHz frequency
  - Over constraining clocks will result in higher dynamic power estimate
- **Specify %high and activity of large fan out control nets**
  - Global set, resets and clock enables

Power Optimization

- Enabling the Power Opt Design option prior to place_design results in a complete power optimization to be performed.
- This option yields the best possible power saving from the Vivado tools
- report_power_opt
- set_power_opt

```
set_power_opt -cell_types bram
set_power_opt -exclude_cells cpuEngine
set_power_opt -include_cells cpuEngine/cpu_dbg_dat_i
power_opt_design
```

DEMO