Vivado从此开始（To Learn Vivado From Here）

本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用

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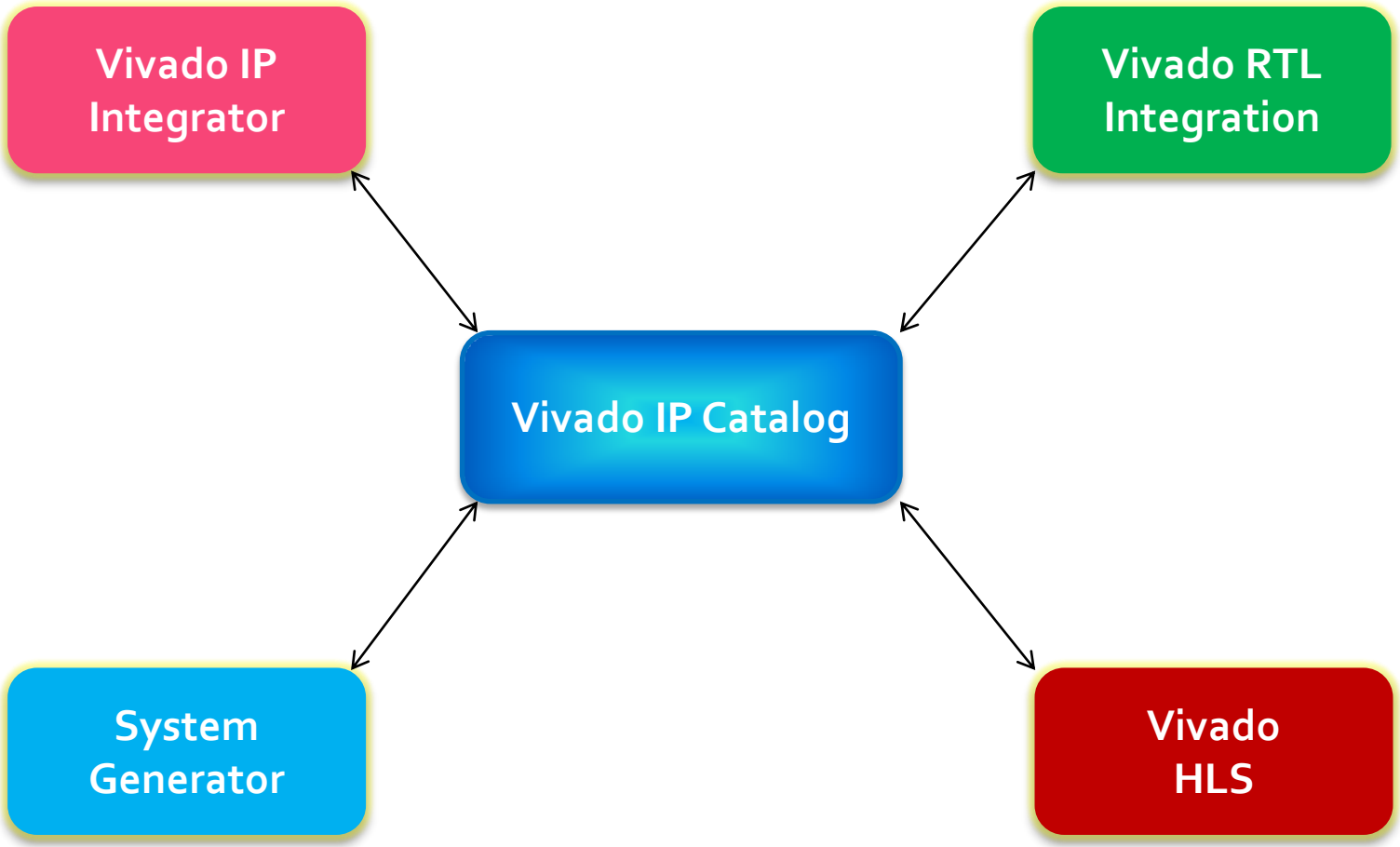
- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

- 内容翔实全面：涵盖Vivado所有基本功能
- 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- 描述图文并茂：给出具体操作步骤，易于快速动手实践

Design With Vivado IP Integrator

Lauren Gao

Complete IP & System Centric Design Flow



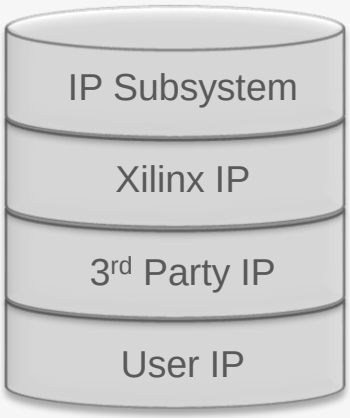
IP Integrator

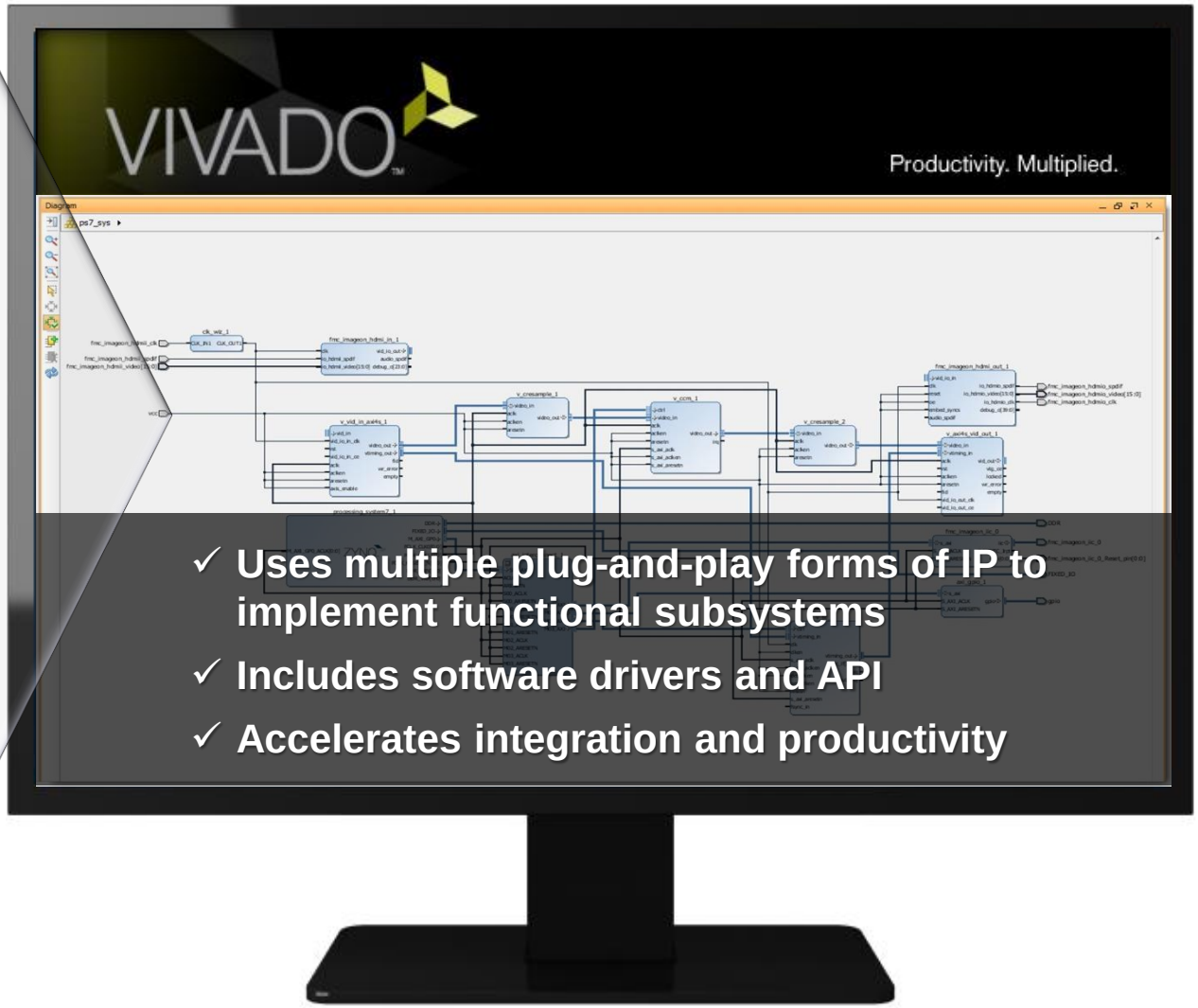
Enabling Reuse and Delivering Fully Functional IP Subsystems

IP Packager

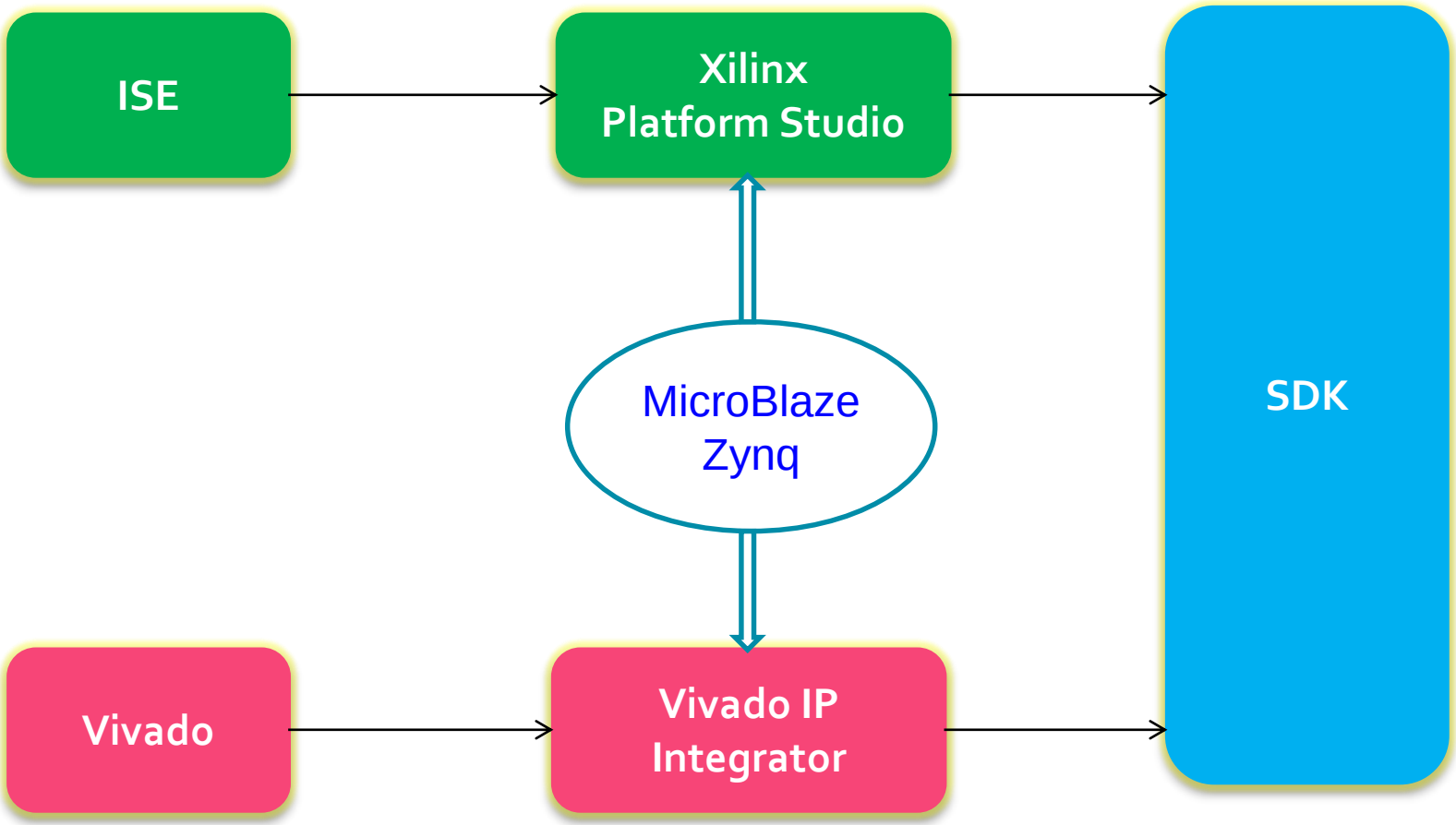
- Source (C, RTL, IP)
- Simulation models
- Documentation
- Example Designs
- Test bench

Standardized IP-XACT

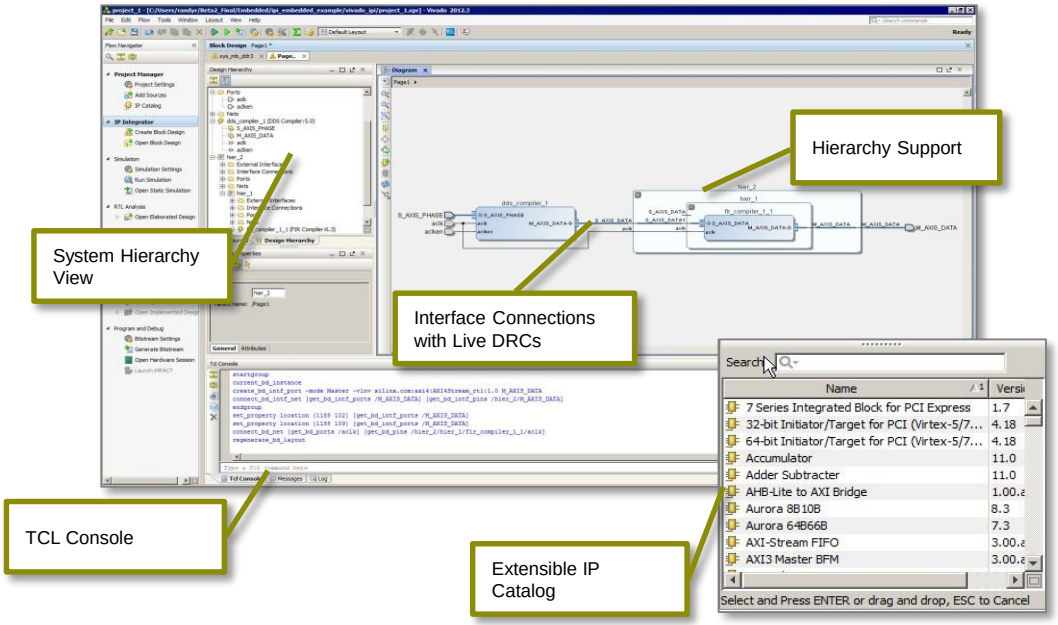




Embedded Processor Hardware Design

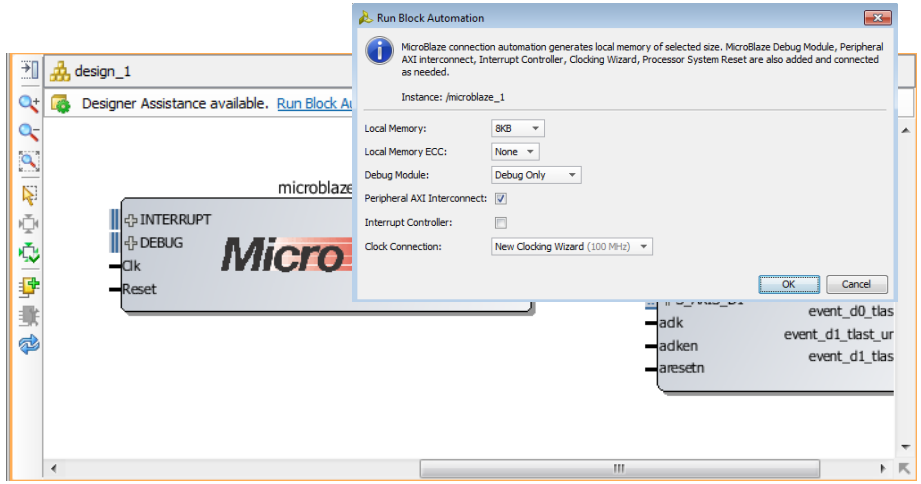


Vivado IP Integrator: Intelligent IP Integration

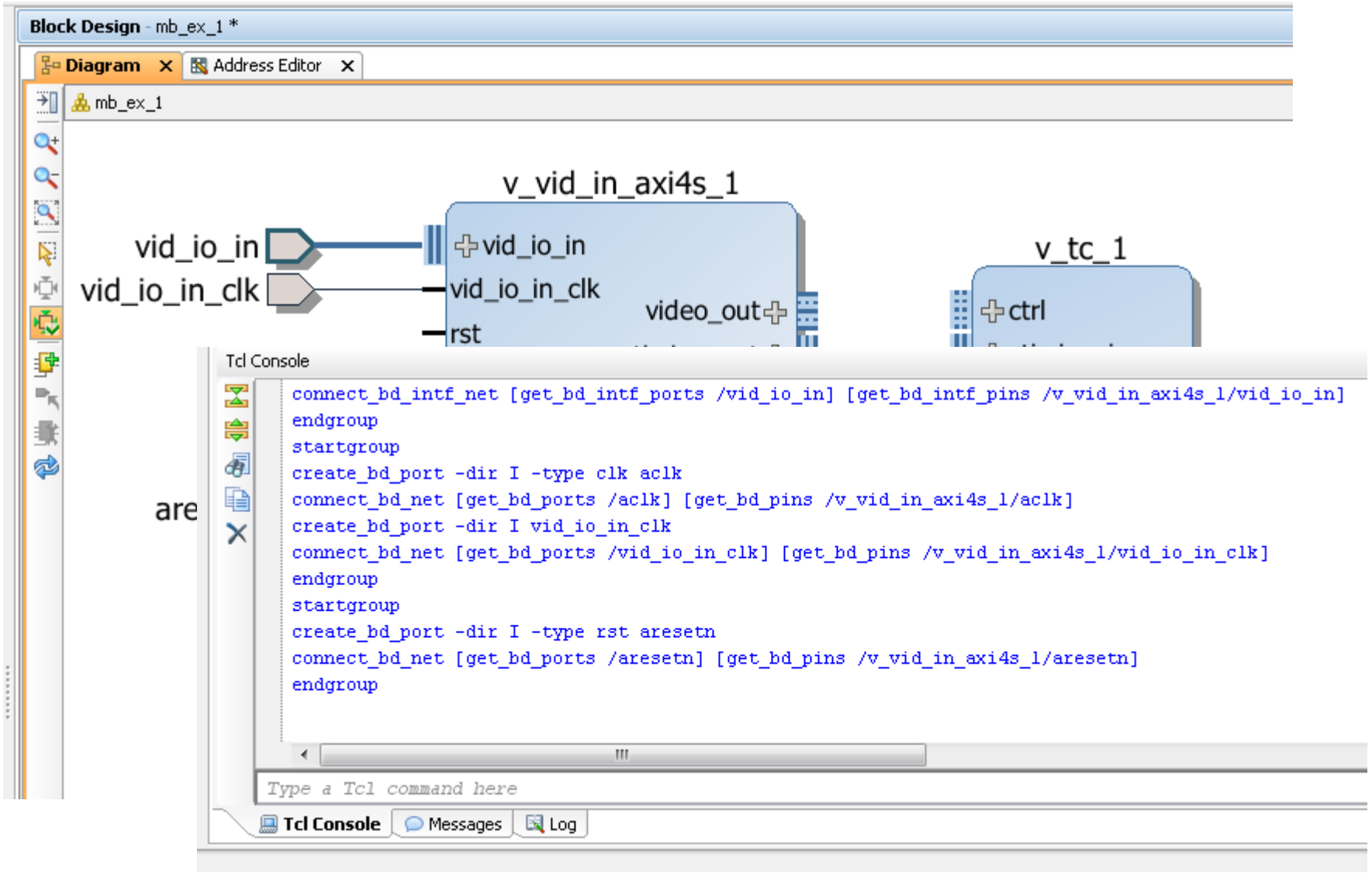


- **Correct-by-construction**
  - Extensible IP repository
  - Real-time DRCs and parameter propagation/resolution
  - Designer Assistance

- **Automated IP Subsystems**
  - Block automation for rapid design creation
  - One click IP customization

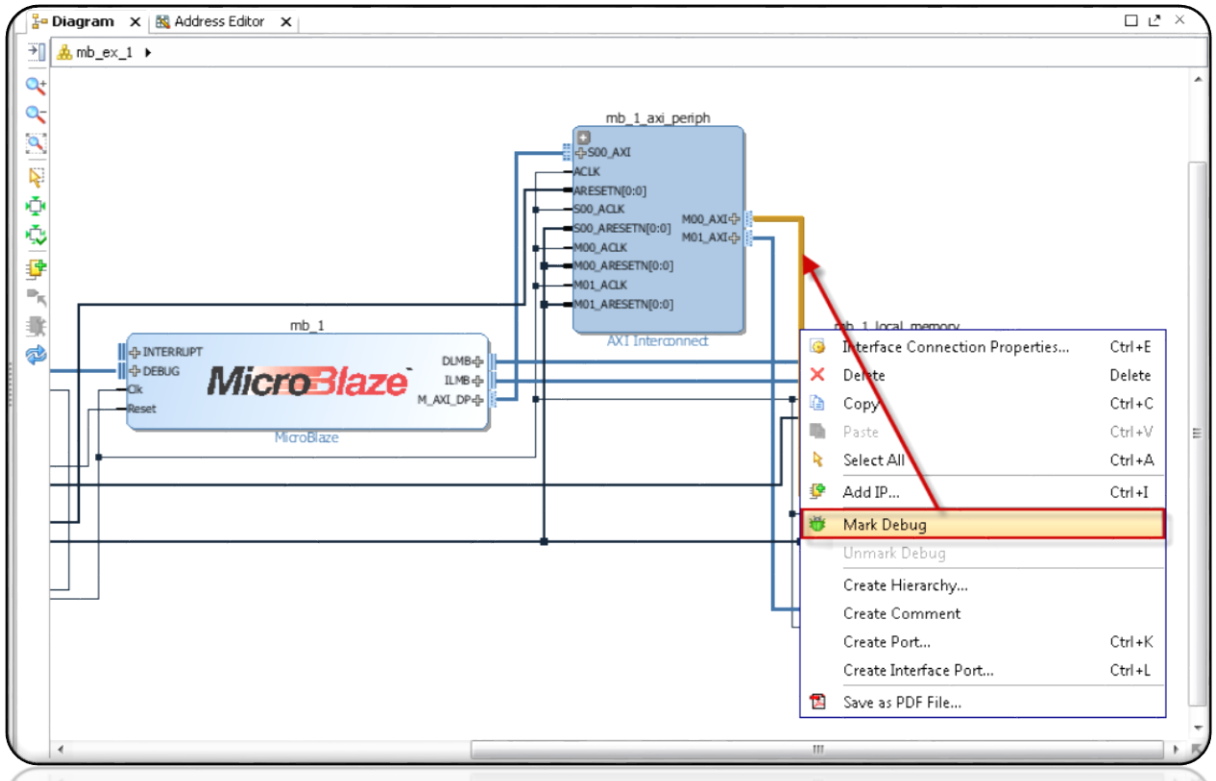


Advanced GUI with full TCL support



Debug support

- **User marks signals or interfaces to debug**
  - This automatically sets up waveforms in HDL simulator to view
  - Also specifies signals to debug in hardware



Vivado IP Integrator Feature

- Run Block Automation
- Run Connection Automation
- Address Editor
- Add MARK_DEBUG
- Regenerate Layout
- Validate Design
- Generate Block Design
- Create HDL Wrapper

Summary

- **Vivado IP integrator**
  - Is platform aware with real-time DRCs
  - Can build and reuse IP subsystems
  - Enables intelligent IP integration
  - Supports integrated debug
  - Full GUI and/or TCL interfaces
  - Raises the level of design abstraction, and increases designer productivity!

DEMO