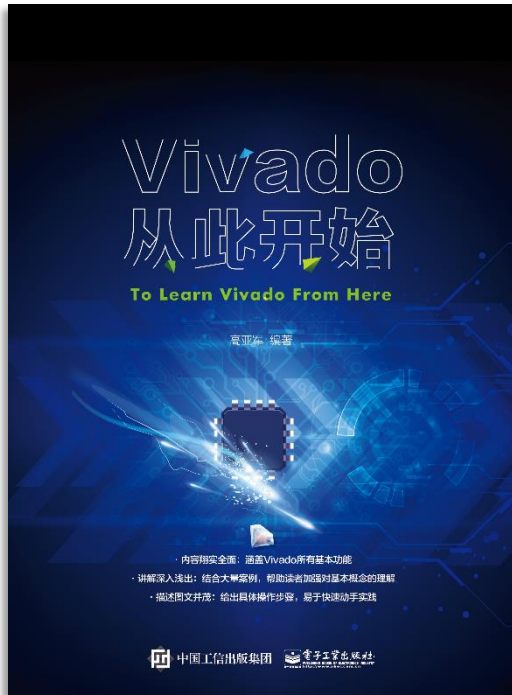


Vivado从此开始 (To Learn Vivado From Here)



本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用



作者：高亚军（Xilinx战略应用高级工程师）

- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

- ◆ 内容翔实全面：涵盖Vivado所有基本功能
- ◆ 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- ◆ 描述图文并茂：给出具体操作步骤，易于快速动手实践



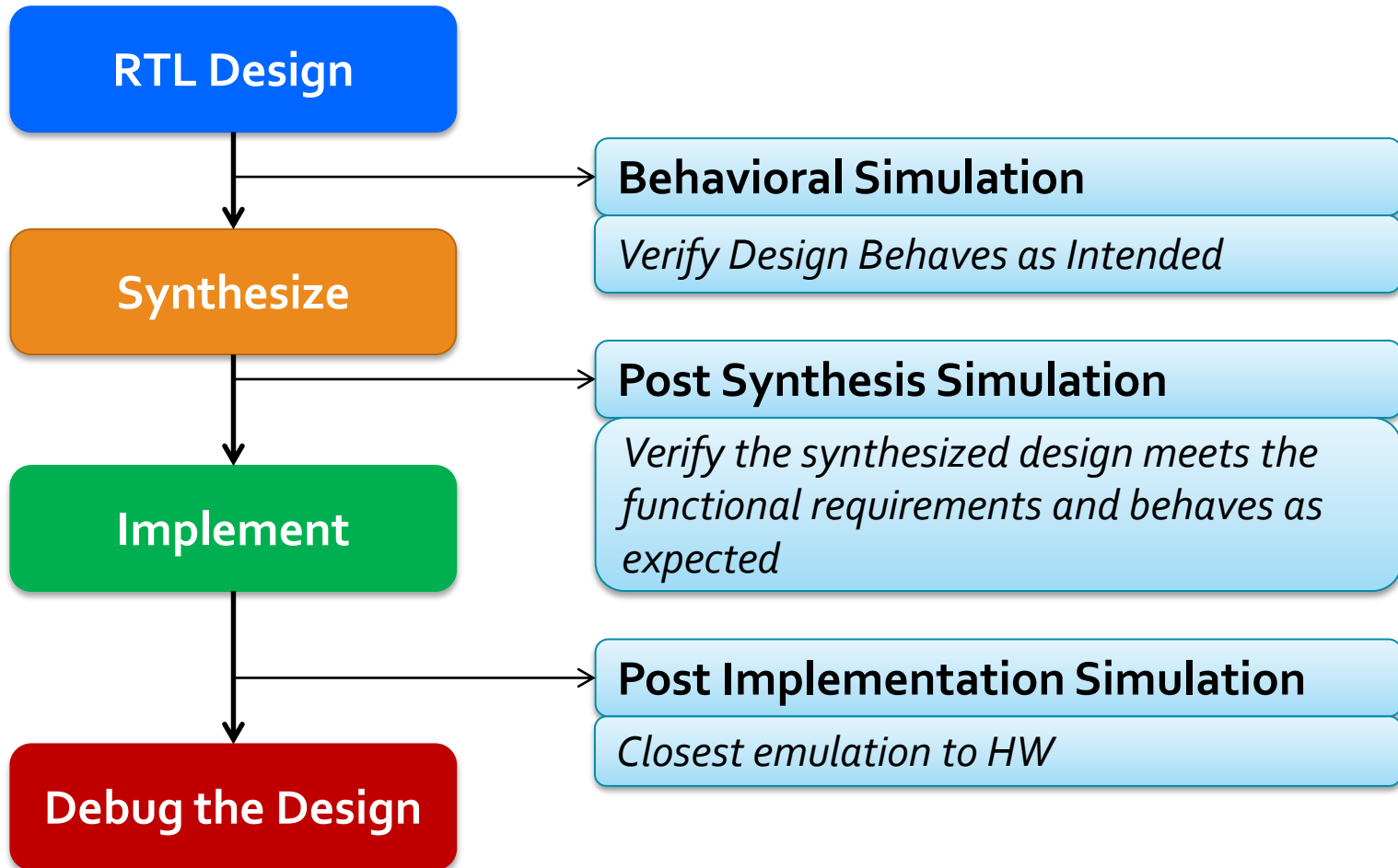
XILINX

ALL PROGRAMMABLE™

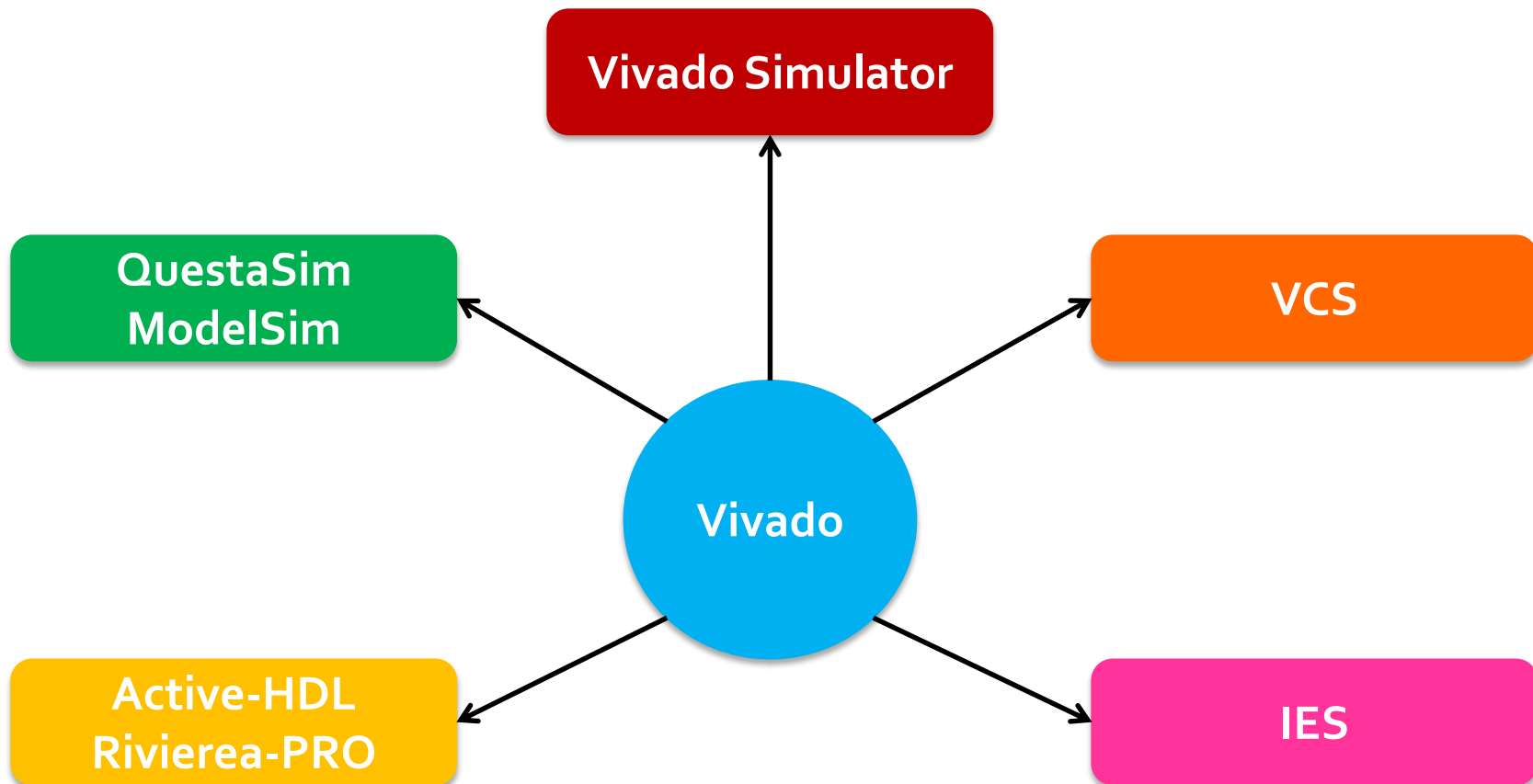
Logic Simulation with XSim

Lauren Gao

Simulation Flow



Vivado Supported Simulators



Simulation libraries are precompiled in the Vivado® Design Suite for use with the Vivado simulator. You must compile libraries when using third party simulators

xsim.ini

<Vivado_Install_Dir>/data/xsim

```
-- Default lib mapping for Simulator
std=$RDI_DATADIR/vhdl/xsim/std
ieee=$RDI_DATADIR/vhdl/xsim/ieee
vl=$RDI_DATADIR/vhdl/xsim/vl
synopsys=$RDI_DATADIR/vhdl/xsim/synopsys
unisim=$RDI_DATADIR/vhdl/xsim/unisim
unimacro=$RDI_DATADIR/vhdl/xsim/unimacro
unifast=$RDI_DATADIR/vhdl/xsim/unifast
xilinxcorelib=$RDI_DATADIR/vhdl/xsim/xilinxcorelib
simprims_ver=$RDI_DATADIR/verilog/xsim/simprims_ver
unisims_ver=$RDI_DATADIR/verilog/xsim/unisims_ver
unimacro_ver=$RDI_DATADIR/verilog/xsim/unimacro_ver
unifast_ver=$RDI_DATADIR/verilog/xsim/unifast_ver
xilinxcorelib_ver=$RDI_DATADIR/verilog/xsim/xilinxcorelib_ver
secureip=$RDI_DATADIR/verilog/xsim/securei
```

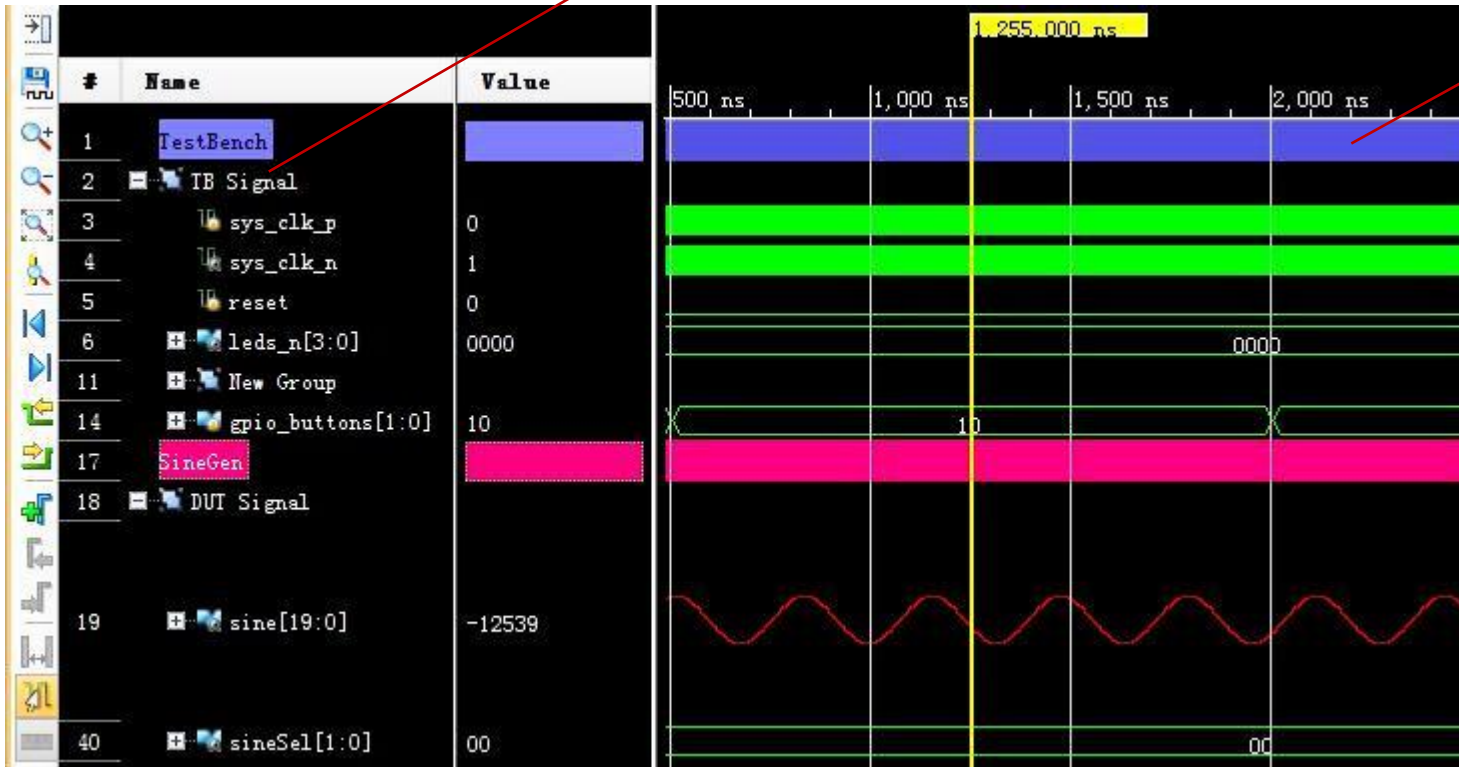
XSim

```
136 else
137 count <= count + 1;
138 sine_h_dly <= sine_h;
```

Add breakpoint in the source code

group

VCD dumping

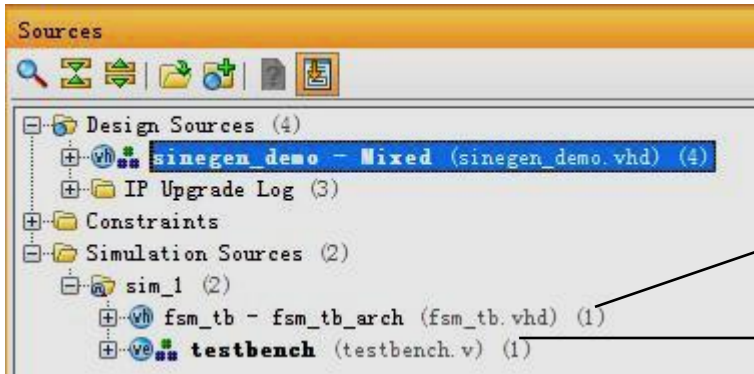


divider

Analog form

Single or Multiple Simulation Sets

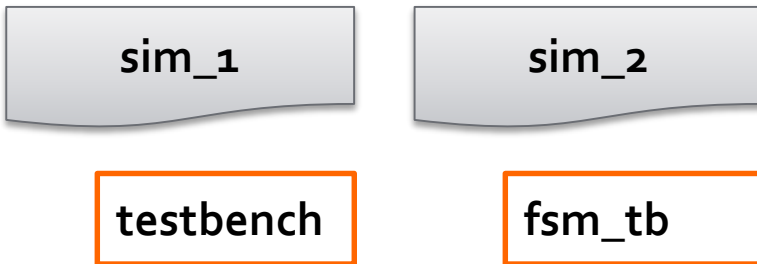
Single Simulation Set



Sub module testbench

Top module testbench

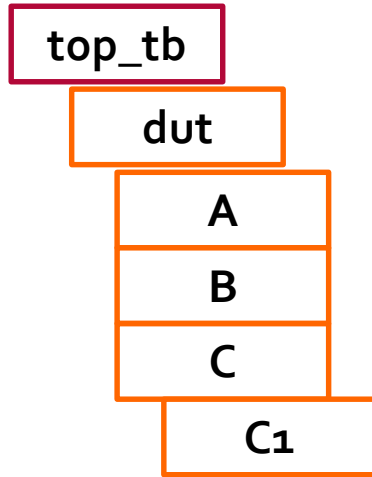
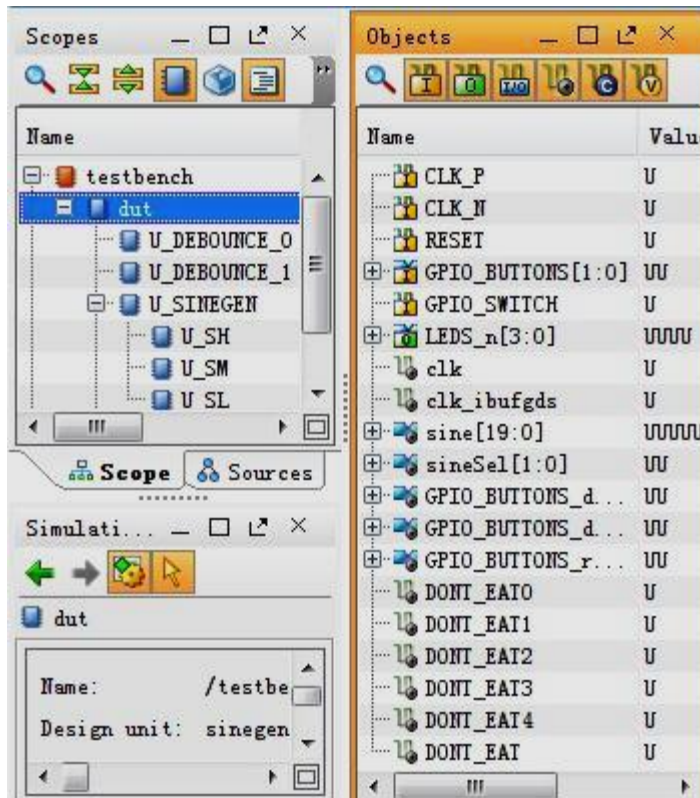
Multiple Simulation Sets



Multiple Simulation Sets

- Using different simulation settings
- Simulation sub modules

Scope & Objects



Each module can be a scope

current_scope
get_scopes
report_scopes

get_objects
report_objects

Scope

- Verilog: module, function, task, process, or begin-end blocks
- VHDL: entity/architecture definitions, block, function, procedure, and process blocks

Objects

- HDL signals, variables, or constants