Vivado从此开始（To Learn Vivado From Here）

本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用

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- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

- 内容翔实全面：涵盖Vivado所有基本功能
- 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- 描述图文并茂：给出具体操作步骤，易于快速动手实践

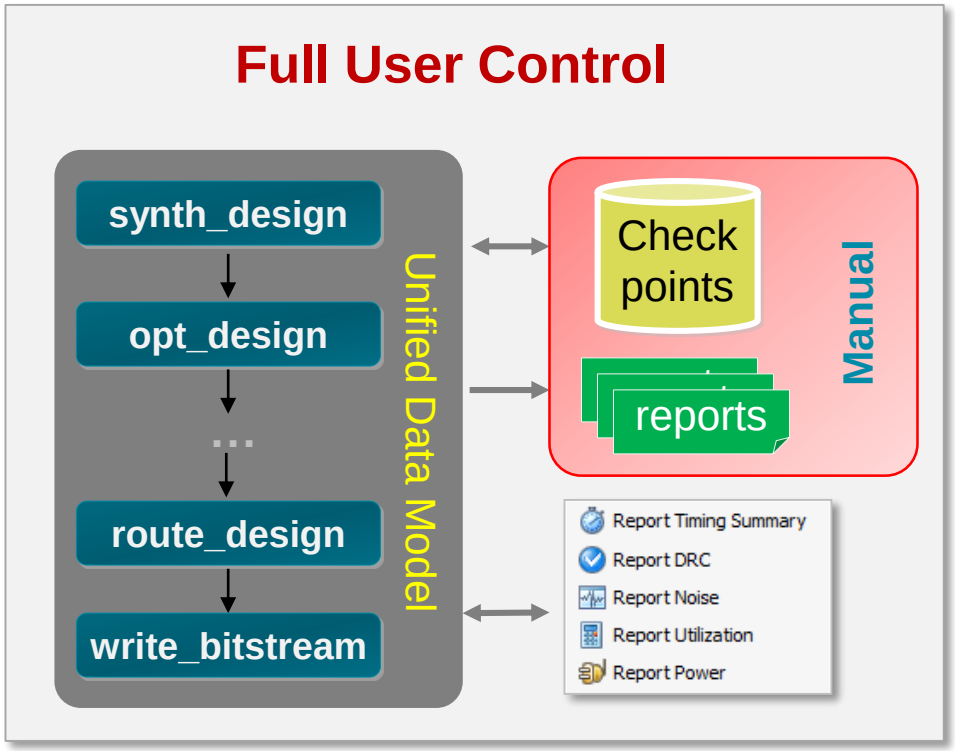
TCL, Vivado One World

Part 7: Design Flow Management with Tcl in Non Project Mode

Lauren Gao

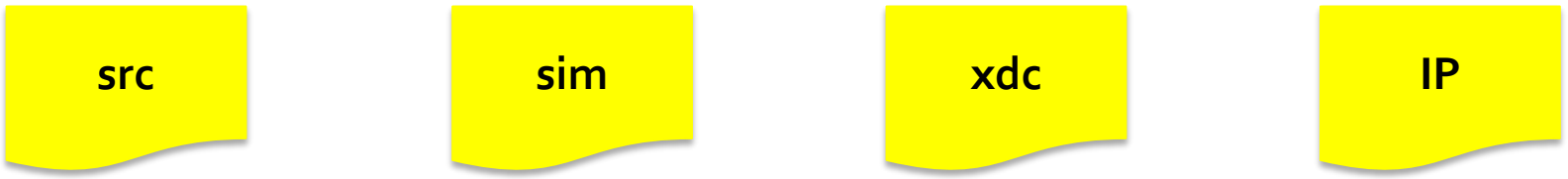
Non-Project Mode – ASIC Type Flow

- **Key advantage – full control over each design flow step**
  - Full freedom and responsibility to manage a design
    - Project status
    - HDL sources, constraints, IPs
    - Dependency management
    - Store results, reports
    - Save checkpoints
    - No automatic multiple-run support
- **Flow control**
  - Synthesis / implementation – Tcl
  - Design analysis – Tcl and/or GUI



Preparing Design Files for Vivado Non Project

- **Four types of design files**
  - RTL design files
    - VHDL (.vhd), Verilog (.v), System Verilog (.sv)
  - XDC files for design constraints
    - .xdc, support both project and module design constraints
  - IP files
    - .xci, IPs have been generated by Vivado Manage IP
    - EDIF or NGC files
- **It's better to create different file folder to store the design files accordingly**



Read Design Files into the In-memory Design

- Read VHDL files
  - `read_vhdl`
- Read Verilog files
  - `read_verilog`
  - For verilog include files

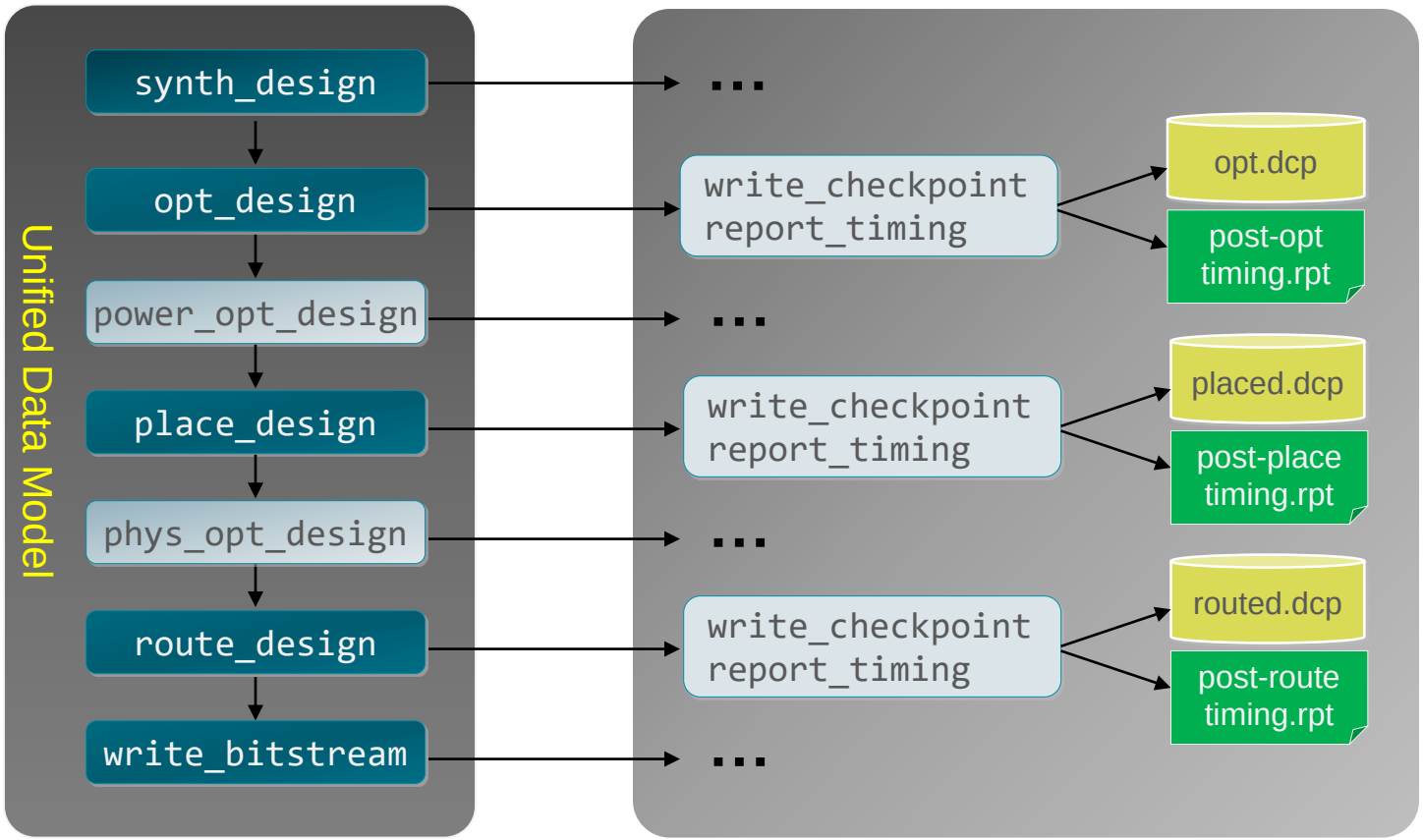
```
set_property FILE_TYPE "Verilog Header" [get_files include.v]
set_property IS_GLOBAL_INCLUDE true [get_files include.v]
```

- Read 3rd party files (EDIF or NGC)
  - `read_edif`
- Read design constraints files
  - `read_xdc`
- Read IP files customized by Vivado
  - `read_ip`
  - All output products associated with the IP core, including the design checkpoint file (DCP) will be read into the in-memory design

Scripted Non-Project Flow

Run Tcl flow commands directly from the Vivado IDE Tcl prompt

Manual results and reports management



Scripted Non-Project Flow: Example

define variables

read sources

synthesis
store results

optimization
placement
store results / reporting
physical optimization

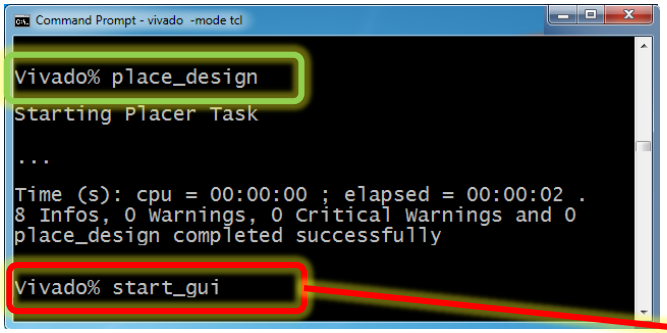
routing
store results / reporting

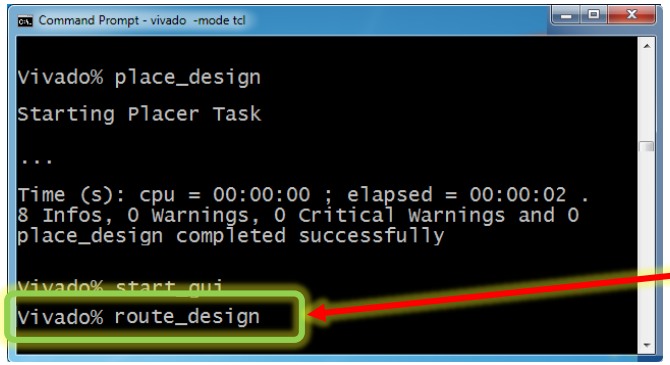
bitstream generation

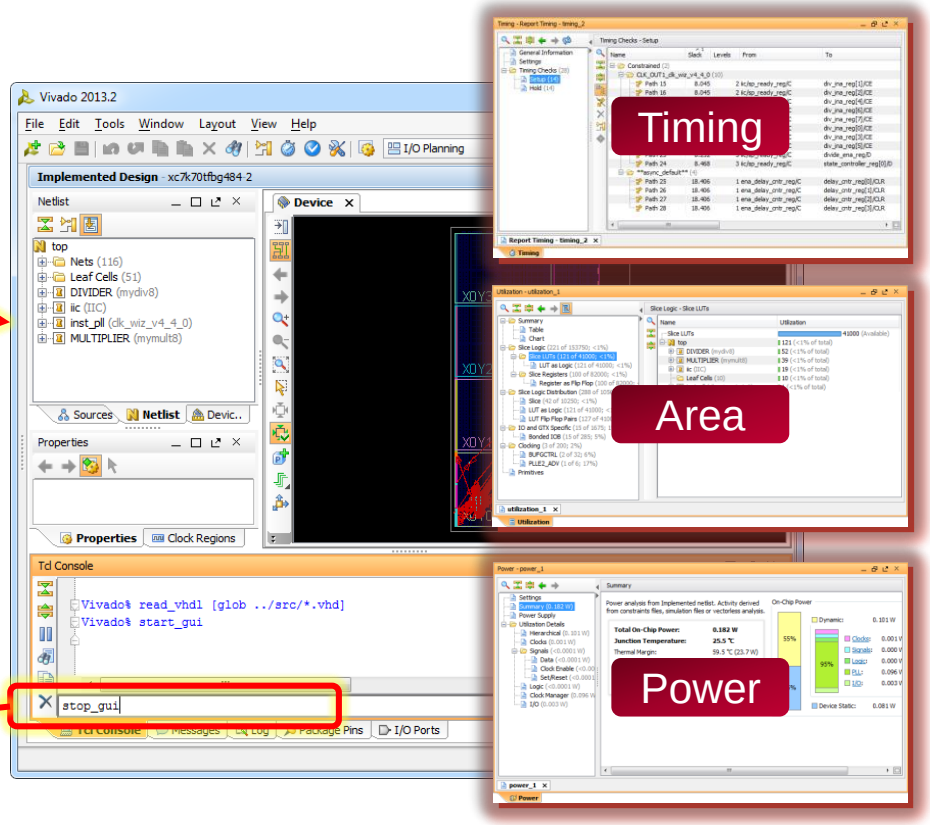
```
set_property      part xc7v485tffbg1157-3
set_property      top
set synthOptions {-flatten_hierarchy}

read_verilog      top.v

synth_design      $synthOptions -top $top -part $part
write_checkpoint synth.dcp

# Emulate Performance_Explore Strategy
opt_design        -directive Explore
place_design      -directive Explore
write_checkpoint placed.dcp
report_timing     -max_paths 100 -file placed.rpt
phys_opt_design   -directive Explore

route_design      -directive Explore
write_checkpoint routed.dcp
report_timing     -max_paths 100 -file routed.rpt

write_bitstream   bitstream.bit
```

Using GUI Design Analysis Features

start_gui / stop_gui







Note: You can continue running route_design from GUI (Tcl Console)

Comparing Project and Non-Project Commands Reference Info

- Key flow commands

Project Tcl Commands	Non-Project Tcl Commands
add_files launch_runs synth_1 wait_on_run synth_1 launch_runs impl_1 wait_on_run impl_1 launch_runs impl_1 – to_step write_bitstream	read_<file type> synth_design; write_checkpoint report_utilization opt_design; write_checkpoint power_opt_design; write_checkpoint place_design; write_checkpoint report_utilization phys_opt_design; write_checkpoint route_design; write_checkpoint report_timing_summary report_power; report_drc write_bitstream file.bit

Some Issues When Using read_ip

Example 1

WARNING: [IP_Flow 19-1100] IP 'blk_mem_gen_v7_3_0' does not match the current project part 'xc7vx485tffg1157-1'. You can continue to use existing outputs but part differences may result in undefined behavior. Please review your project settings if this is unexpected."

An error will result if the IP in use does not support the xc7vx485tffg1157-1 device.

Example 2

"Generating IP 'my_core' ...
Delivering 'Synthesis' files for IP 'My_core'.
Error: [Xilinx.com:ip:mig_7series:2.0-0] my_core: Target FPGA device"xc7k325t' provided by the mig project did not match with the selected FPGA device 'xc7vx485t' in the project settings. Please cross check the MIG project loader or review the project settings"

```
CRITICAL WARNING: [Designutils 20-1365] Unable to generate target(s) for the following file is locked
```

or

```
WARNING: [IP_Flow 19-2162] IP '...' is locked. Locked reason: IP '...' is write protected.
...
WARNING: [Common 17-259] Unknown Tcl command
```

or

```
ERROR:sim:709 - Unable to migrate project
...
ERROR: [IP_Flow 19-98] Generation of the IP CORE failed.
```

Solution

```
create_project -in memory
set_property part <part> [current_project]
read_ip <xci file>
set_property is_locked false [get_files <xci file>]
generate_target synthesis [get_files <xci file>]
synth_design -top <top name> -part <part>
```

Demo