Vivado从此开始（To Learn Vivado From Here）

本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用

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- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

- 内容翔实全面：涵盖Vivado所有基本功能
- 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- 描述图文并茂：给出具体操作步骤，易于快速动手实践

Logic Simulation with ModelSim

Lauren Gao

Compile Xilinx Simulation Library

- **compile_simlib**
  - ✓ **-directory**
    - Directory path for saving the compiled results
  - ✓ **-family**
    - virtex7, kintex7, kintex7l, artix7, artix7l, zynq, default: all
  - ✓ **-language**
    - vhdl, verilog, default: all
  - ✓ **-library**
    - Unisim, simprim, xilinxcorelib, edk, default: all
  - ✓ **-simulator**
    - modelsim, questa, ies, vcs_mx, riviera, active_hdl
  - ✓ **-simulator_exec_path**
    - ModelSim: E:\modeltech64_10.2\win64
  - ✓ **-32bit**
    - Perform simulator compilation in 32-bit mode instead of the default 64-bit compilation

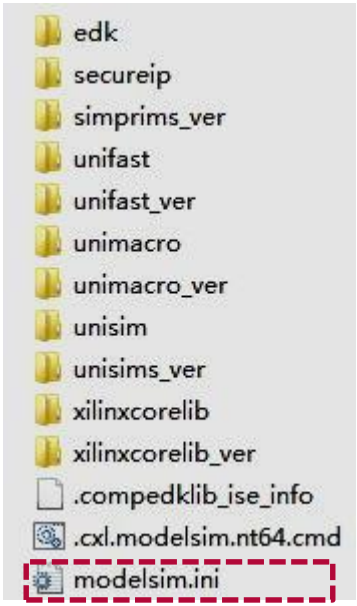
Use ModelSim as 3rd Party Simulator

```
set target_dir {E:\Xilinx\Xlib}
set sim_exe_path {E:\modeltech64_10.2\win64}
compile_simlib -directory $target_dir -family all -language all \
-library all -simulator modelsim -simulator_exec_path $sim_exe_path
```

- **Where can run it**
  - In Vivado Tcl console
  - In Vivado Tcl shell
- **When to run it**
  - Anytime a new simulator version is installed
  - Anytime a new version of Vivado IDE is installed
- **How to run it**
  - Single command step by step
  - As Tcl file, use source command

Compilation Summary

```
Copying setup file 'modelsim.ini' to 'E:\Xilinx\Xlib/modelsim.ini' ...
*******************************************************************************
*                          COMPILATION SUMMARY                                *
*                                                                             *
*  Simulator used: modelsim                                                   *
*  Compiled on: Thu Nov 21 14:49:35 2013                                      *
*                                                                             *
*******************************************************************************
*          Library          | Lang    | Mapped Name(s)   | Err#(s) | Warn#(s) *
*-----------------------------------------------------------------------------*
*  secureip                 | verilog | secureip         | 0       | 0        *
*-----------------------------------------------------------------------------*
*  unisim                   | vhdl    | unisim           | 0       | 0        *
*-----------------------------------------------------------------------------*
*  unisim                   | verilog | unisims_ver      | 0       | 0        *
*-----------------------------------------------------------------------------*
*  simprim                  | verilog | simprims_ver     | 0       | 0        *
*-----------------------------------------------------------------------------*
*  xilinxcorelib            | vhdl    | xilinxcorelib    | 0       | 357      *
*-----------------------------------------------------------------------------*
*  xilinxcorelib            | verilog | xilinxcorelib_ver| 0       | 1        *
*-----------------------------------------------------------------------------*
*  edk                      |         | edk              | 0       | 183      *
*-----------------------------------------------------------------------------*
```



Should We Compile Simulation Library for Different Project?

NO

Why?

Set compiled library as global library

modelsim.ini

```
3 ; All Rights Reserved.
4 ;
5 ; THIS WORK CONTAINS TRADE SECRET AND
  PROPRIETARY INFORMATION WHICH IS THE
  PROPERTY OF
6 ; MENTOR GRAPHICS CORPORATION OR ITS
  LICENSORS AND IS SUBJECT TO LICENSE TERMS.
7 ;
8
9 [Library]
10 others = $MODEL_TECH/../modelsim.ini
11 ;
12 ; VITAL concerns:
```