Vivado从此开始（To Learn Vivado From Here）

本书围绕Vivado四大主题

- 设计流程
- 时序约束
- 时序分析
- Tcl脚本的使用

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- 2012年2月，出版《基于FPGA的数字信号处理（第1版）》
- 2012年9月，发布网络视频课程《Vivado入门与提高》
- 2015年7月，出版《基于FPGA的数字信号处理（第2版）》
- 2016年7月，发布网络视频课程《跟Xilinx SAE学HLS》

- 内容翔实全面：涵盖Vivado所有基本功能
- 讲解深入浅出：结合大量案例，帮助读者加强对基本概念的理解
- 描述图文并茂：给出具体操作步骤，易于快速动手实践

Incremental Implementation

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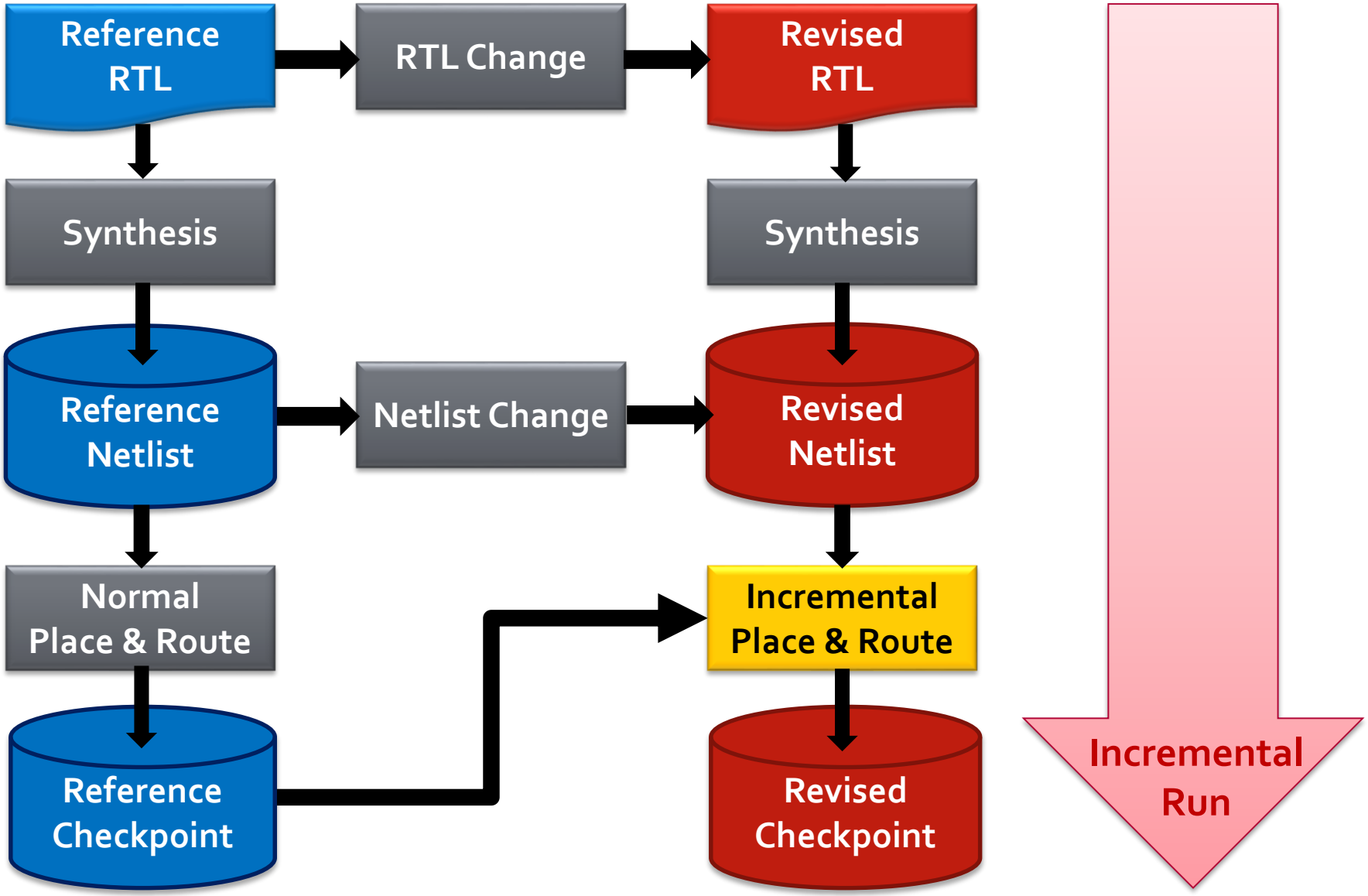
Agenda

- Basic Incremental Compile Flow
- Running Incremental Compile in Project Mode and Non-Project Mode
- Advanced Analysis for Incremental Compile
- Demo

Incremental Compile Flow



When and Why to Use Incremental Flow

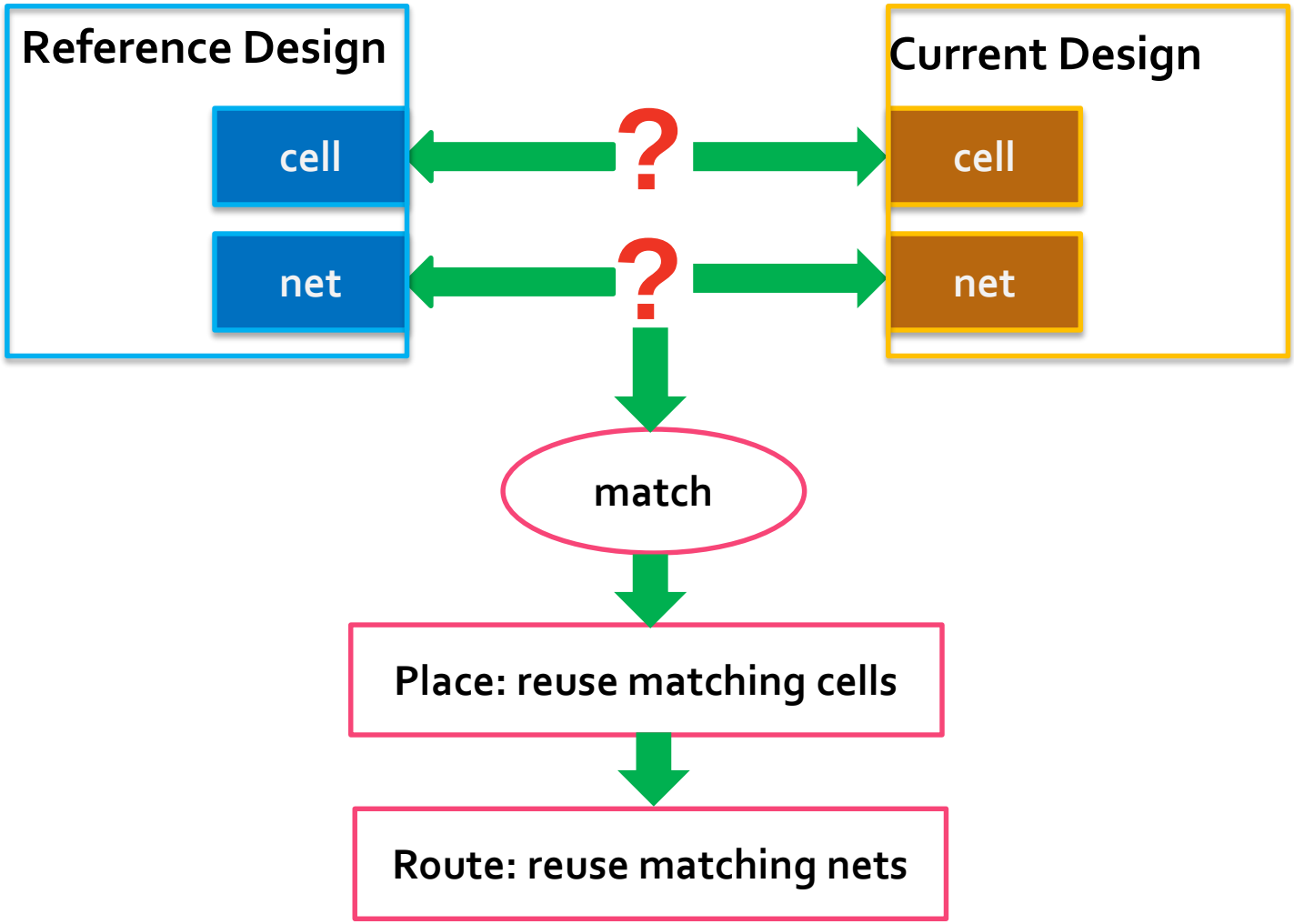
- **When**
  - Less than 5% change in cells ➔ 3x speedup in P&R runtime
- **Why**
  - Save runtime
  - More predictable results
  - Faster timing closure

Reuse existing design data after small RTL changes
Do not use the incremental flow after major design changes

Reference Design & Current Design

- **Reference design**
  - An earlier iteration or variation of the current design
  - It has been synthesized, placed and routed
  - What we use as reference is <_routed.dcp>
- **Current design**
  - The current design incorporates small design changes or variations from the reference design
  - These changes or variations can include
    - RTL changes
    - Netlist changes
    - Both RTL changes and netlist changes

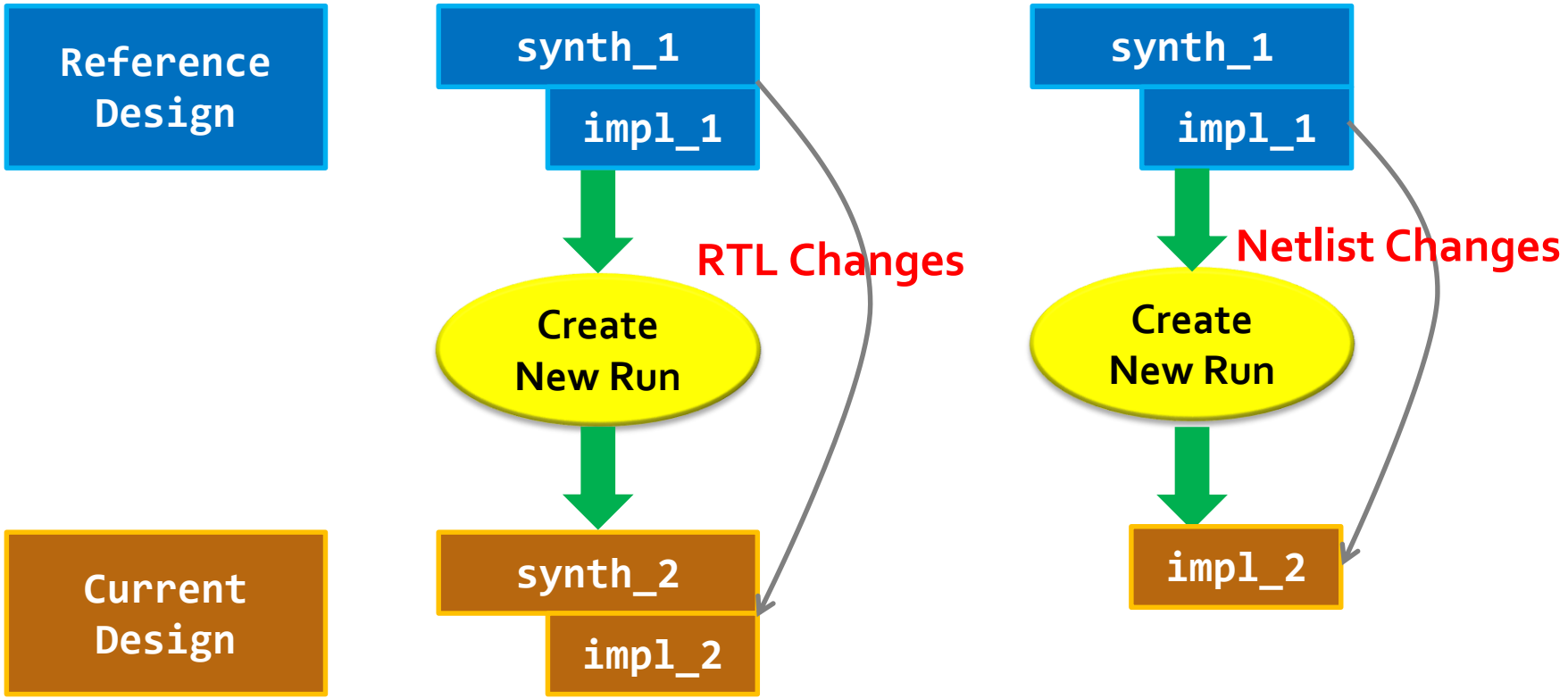
Running Incremental Place and Route



Effectively Reusing Placement and Routing

- **the following can have a large impact on incremental placement and routing runtime**
  - Impact of small RTL changes: the following can lead to very large changes in the synthesized netlist
    - Increasing the size of an inferred memory
    - Widening an internal bus
    - Changing data types from unsigned to signed
  - Impact of changing constraints and synthesis options
    - Changing timing constraints and resynthesizing
    - Preserving or dissolving logical hierarchy
    - Enabling register re-timing

Original Run and New Run



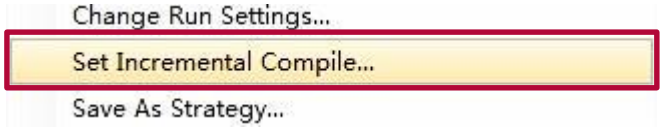
- Both runs have the same strategy
- -directive cannot be used in incremental mode
- phys_opt_design does not have an incremental mode

```
WARNING: [Vivado_Tcl 4-205] '-directive' option will be ignored since it is currently not supported with incremental place_design
WARNING: [Vivado_Tcl 4-206] '-directive' option will be ignored since it is currently not supported with incremental route_design
```

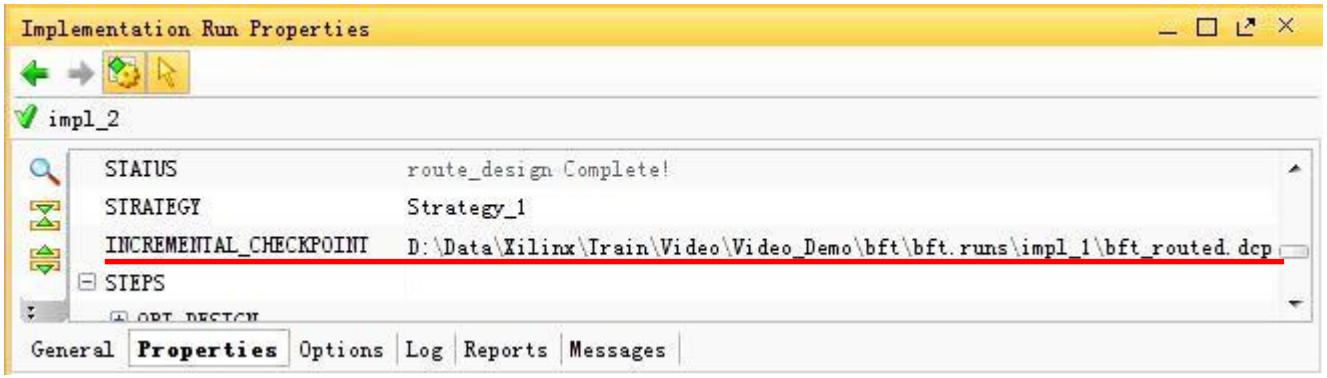
Using Incremental Compile in Project Mode

- Implementation settings → incremental compile

- Select the run and apply a reference checkpoint



- After select incremental compile, it can be shown in run property

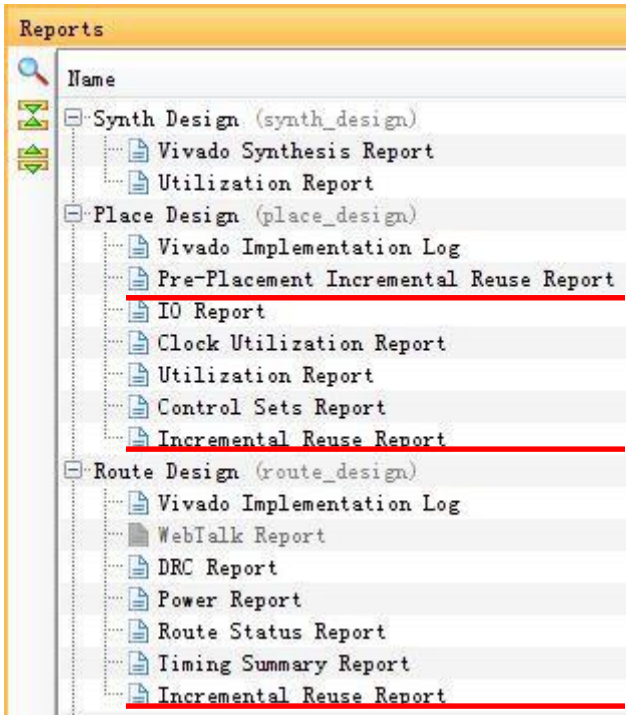



```
set_property INCREMENTAL_CHECKPOINT reference.dcp [get_runs impl_2]
```

Using Incremental Compile in Non-Project Mode

```
# read revised design
link_design -part $my_part -top $revised_top
opt_design
read_checkpoint -incremental $ref.dcp
place_design
# if run in original, reference run
phys_opt_design
route_design
report_incremental_reuse -file routed_reuse.rpt
report_timing_summary -label_reused -max_paths 10 \
–file routed_ts.rpt
```

Incremental Reuse Report




```
1. Netlist Similarity Summary
-----------------------------

+---------------+-------+-------+------------+
|      Type     | Count | Total | Percentage |
+---------------+-------+-------+------------+
| Matched Cells |  3609 |  3617 |      99.77 |
| Matched Ports |    71 |    71 |     100.00 |
| Matched Nets  |  6154 |  6170 |      99.74 |
+---------------+-------+-------+------------+
```

```
2. Implementation Reuse Summary
-------------------------------

+-----------------------------------------------------+-------+-------+------------+
|                         Type                        | Count | Total | Percentage |
+-----------------------------------------------------+-------+-------+------------+
| Reused Cells                                        |  3607 |  3617 |      99.72 |
| Reused Ports                                        |    71 |    71 |     100.00 |
| Reused Nets                                         |  5137 |  5153 |      99.68 |
|                                                     |       |       |            |
| Non-Reused Cells                                    |    10 |  3617 |       0.27 |
|   New                                               |     8 |  3617 |       0.22 |
|   Discarded illegal placement due to netlist changes |     2 |  3617 |       0.05 |
| Fully Reused nets                                   |  4764 |  5153 |      92.45 |
| Partially reused nets                               |   373 |  5153 |       7.23 |
| Non-Reused nets                                     |    16 |  5153 |       0.31 |
+-----------------------------------------------------+-------+-------+------------+
```

Advanced Analysis

- report_timing/report_timing_summary –label_reused

```
-------------------------------------------------------------------    -------------------
 (R)SLICE_X39Y35      FDCE (Prop_fdce_C_Q)         0.100     1.665 r  egressLoop[1].egressFifo/
                      net (fo=3, routed)           0.224     1.889    egressLoop[1].egressFifo/
 (R)SLICE_X41Y35                                                   r  egressLoop[1].egressFifo/
 (PNR)SLICE_X41Y35    LUT6 (Prop_lut6_I2_O)        0.028     1.917 r  egressLoop[1].egressFifo/
                      net (fo=1, routed)           0.000     1.917    egressLoop[1].egressFifo/
 (PNR)SLICE_X41Y35                                                 r  egressLoop[1].egressFifo/
 (R)SLICE_X41Y35      CARRY4 (Prop_carry4_S[1]_CO[3])
                                                   0.114     2.031 r  egressLoop[1].egressFifo/
                      net (fo=1, routed)           0.254     2.285    egressLoop[1].egressFifo/
 (R)SLICE_X38Y34                                                   r  egressLoop[1].egressFifo/
 (PNR)SLICE_X38Y34    LUT4 (Prop_lut4_I2_O)        0.100     2.385 r  egressLoop[1].egressFifo/
                      net (fo=1, routed)           0.000     2.385    egressLoop[1].egressFifo/
 (PNR)SLICE_X38Y34    FDPE                                         r  egressLoop[1].egressFifo/
-------------------------------------------------------------------    -------------------
```

(R)	Both the cell placement and net routing are reused
(NR)	Neither the cell placement nor the net routing are reused
(PNR)	The cell placement is reused but the net routing is not reused
(N)	The pin, cell, or net is a new design object

Advanced Analysis

```
get_property INCREMENTAL_CHECKPOINT [current_run]
reset_property

set myreused_cells [get_cells -hier -filter "IS_REUSED == TRUE"]
report_property [lindex $myreused_cells 0]

set myreused_nets [get_nets -hier -filter "IS_REUSED == TRUE"]
report_property [lindex $myreused_nets 0]

set myreused_pins [get_pins -hier -filter "IS_REUSED == TRUE"]
report_property [lindex $myreused_pins 0]

set myreused_ports [get_ports -filter "IS_REUSED == TRUE"]
report_property [lindex $myreused_ports 0]
```

Demo